1.55V DDR2 SDRAM FBDIMM

MT18RTF25672FDZ – 2GB

Features

- 240-pin, fully buffered DIMM (FBDIMM)
- Very low-power DDR2 operation
- Component configuration: 256 Meg x 8
- 1.5V ≤ V_{DD} ≤ 1.9V for DDR2 SDRAM
- 1.5V ≤ V_{DD} ≤ 1.9V for advanced memory buffer (AMB) DRAM I/O
- V_{DD} = 1.55V
- Backward compatible with systems designed for the standard (1.8V) FBDIMM
- Dual rank
- Halogen-free

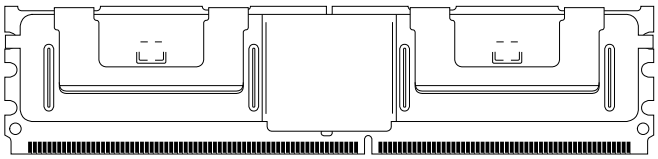
Functionality

This 1.55V FBDIMM consumes less power than a standard 1.8V FBDIMM. However, it has the same timing and operating parameters as a standard FBDIMM. This enables backward compatibility with systems designed for use with standard FBDIMMs.

Information in the 1.8V DDR2 FBDIMM data sheet is directly applicable to this 1.55V DDR2 FBDIMM, except where stated otherwise in this data sheet.

Figure 1: 240-Pin FBDIMM (MO-256 R/C B)

Module height: 30.35mm (1.19in)



Options	Marking
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CL[1]	
– 3.0ns @ CL = 5 (DDR2-667)	-667

Note: 1. CL = CAS (READ) latency.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 5	CL = 4	CL = 3			
-667	PC2-5300	667	553	400	15	15	55
-53E	PC2-4200	–	553	400	15	15	55

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Table 2: Addressing

Parameter	2GB
Refresh count	8K
Device bank address	8 BA[2:0]
Device page size per bank	1KB
Device configuration	1Gb (256 Meg x 8)
Row address	16K A[13:0]
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

Table 3: Part Numbers and Timing Parameters – 2GB

Base device: MT47R128M8,[1] 1Gb DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL -^{t}RCD -^{t}RP)	Link Transfer Rate
MT18RTF25672FDZ-667__	2GB	256 Meg x 72	PC2-5300	3.0ns/667 MT/s	5-5-5	4.0 GT/s

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a four-place code (not shown) that designates component, AMB vendor, and PCB revisions. Consult factory for current revision codes. Example: MT18RTF25672FDZ-667H1D6.

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Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin FBDIMM Front								240-Pin FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{DD}	31	PN3	61	PN9#	91	PS9#[1]	121	V_{DD}	151	SN3	181	SN9#	211	SS9#[1]
2	V_{DD}	32	PN3#	62	V_{SS}	92	V_{SS}	122	V_{DD}	152	SN3#	182	V_{SS}	212	V_{SS}
3	V_{DD}	33	V_{SS}	63	PN10	93	PS5	123	V_{DD}	153	V_{SS}	183	SN10	213	SS5
4	V_{SS}	34	PN4	64	PN10#	94	PS5#	124	V_{SS}	154	SN4	184	SN10#	214	SS5#
5	V_{DD}	35	PN4#	65	V_{SS}	95	V_{SS}	125	V_{DD}	155	SN4#	185	V_{SS}	215	V_{SS}
6	V_{DD}	36	V_{SS}	66	PN11	96	PS6	126	V_{DD}	156	V_{SS}	186	SN11	216	SS6
7	V_{DD}	37	PN5	67	PN11#	97	PS6#	127	V_{DD}	157	SN5	187	SN11#	217	SS6#
8	V_{SS}	38	PN5#	68	V_{SS}	98	V_{SS}	128	V_{SS}	158	SN5#	188	V_{SS}	218	V_{SS}
9	V_{CC}	39	V_{SS}	69	V_{SS}	99	PS7	129	V_{CC}	159	V_{SS}	189	V_{SS}	219	SS7
10	V_{CC}	40	PN13[1]	70	PS0	100	PS7#	130	V_{CC}	160	SN13[1]	190	SS0	220	SS7#
11	V_{SS}	41	PN13#[1]	71	PS0#	101	V_{SS}	131	V_{SS}	161	SN13#[1]	191	SS0#	221	V_{SS}
12	V_{CC}	42	V_{SS}	72	V_{SS}	102	PS8	132	V_{CC}	162	V_{SS}	192	V_{SS}	222	SS8
13	V_{CC}	43	V_{SS}	73	PS1	103	PS8#	133	V_{CC}	163	V_{SS}	193	SS1	223	SS8#
14	V_{SS}	44	DNU	74	PS1#	104	V_{SS}	134	V_{SS}	164	DNU	194	SS1#	224	V_{SS}
15	V_{TT}	45	DNU	75	V_{SS}	105	DNU	135	V_{TT}	165	DNU	195	V_{SS}	225	DNU
16	DNU	46	V_{SS}	76	PS2	106	DNU	136	VID0	166	V_{SS}	196	SS2	226	DNU
17	RESET#	47	V_{SS}	77	PS2#	107	V_{SS}	137	M_TEST (DNU)	167	V_{SS}	197	SS2#	227	V_{SS}
18	V_{SS}	48	PN12[1]	78	V_{SS}	108	V_{DD}	138	V_{SS}	168	SN12[1]	198	V_{SS}	228	SCK
19	DNU	49	PN12#[1]	79	PS3	109	V_{DD}	139	DNU	169	SN12#[1]	199	SS3	229	SCK#
20	DNU	50	V_{SS}	80	PS3#	110	V_{SS}	140	DNU	170	V_{SS}	200	SS3#	230	V_{SS}
21	V_{SS}	51	PN6	81	V_{SS}	111	V_{DD}	141	V_{SS}	171	SN6	201	V_{SS}	231	V_{DD}
22	PN0	52	PN6#	82	PS4	112	V_{DD}	142	SN0	172	SN6#	202	SS4	232	V_{DD}
23	PN0#	53	V_{SS}	83	PS4#	113	V_{DD}	143	SN0#	173	V_{SS}	203	SS4#	233	V_{DD}
24	V_{SS}	54	PN7	84	V_{SS}	114	V_{SS}	144	V_{SS}	174	SN7	204	V_{SS}	234	V_{SS}
25	PN1	55	PN7#	85	V_{SS}	115	V_{DD}	145	SN1	175	SN7#	205	V_{SS}	235	V_{DD}
26	PN1#	56	V_{SS}	86	DNU	116	V_{DD}	146	SN1#	176	V_{SS}	206	DNU	236	V_{DD}
27	V_{SS}	57	PN8	87	DNU	117	V_{TT}	147	V_{SS}	177	SN8	207	DNU	237	V_{TT}
28	PN2	58	PN8#	88	V_{SS}	118	SA2	148	SN2	178	SN8#	208	V_{SS}	238	V_{DDSPD}
29	PN2#	59	V_{SS}	89	V_{SS}	119	SDA	149	SN2#	179	V_{SS}	209	V_{SS}	239	SA0
30	V_{SS}	60	PN9	90	PS9[1]	120	SCL	150	V_{SS}	180	SN9	210	SS9[1]	240	SA1

Note: 1. The following signals are cyclical redundancy code (CRC) bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, and SS9/SS9#.

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Table 5: Pin Descriptions

Symbol	Type	Description
PS[9:0]	Input	Primary southbound data, positive lines.
PS#[9:0]	Input	Primary southbound data, negative lines.
SCK	Input	System clock input, positive line.
SCK#	Input	System clock input, negative line.
SCL	Input	Serial presence-detect (SPD) clock input.
SS[9:0]	Input	Secondary southbound data, positive lines.
SS#[9:0]	Input	Secondary southbound data, negative lines.
PN[13:0]	Output	Primary northbound data, positive lines.
PN#[13:0]	Output	Primary northbound data, negative lines.
SN[13:0]	Output	Secondary northbound data, positive lines.
SN#[13:0]	Output	Secondary northbound data, negative lines.
VID0	Output	Voltage identification, connected to V_{SS}. Indicates 1.5V DRAM present on module.
SA[2:0]	I/O	SPD address inputs, also used to select the FBDIMM number in the AMB.
SDA	I/O	SPD data input/output.
RESET#	Supply	AMB reset signal.
V_{CC}	Supply	AMB core power and AMB channel interface power (1.5V).
V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.5V).
V_{TT}	Supply	DRAM clock, command, and address termination power (V_{DD}/2).
V_{DDSPD}	Supply	SPD/AMB SMBus power.
V_{SS}	Supply	Ground.
M_TEST	–	The M_TEST pin provides an external connection for testing the margin of V_{REF}, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
DNU	–	Do not use.

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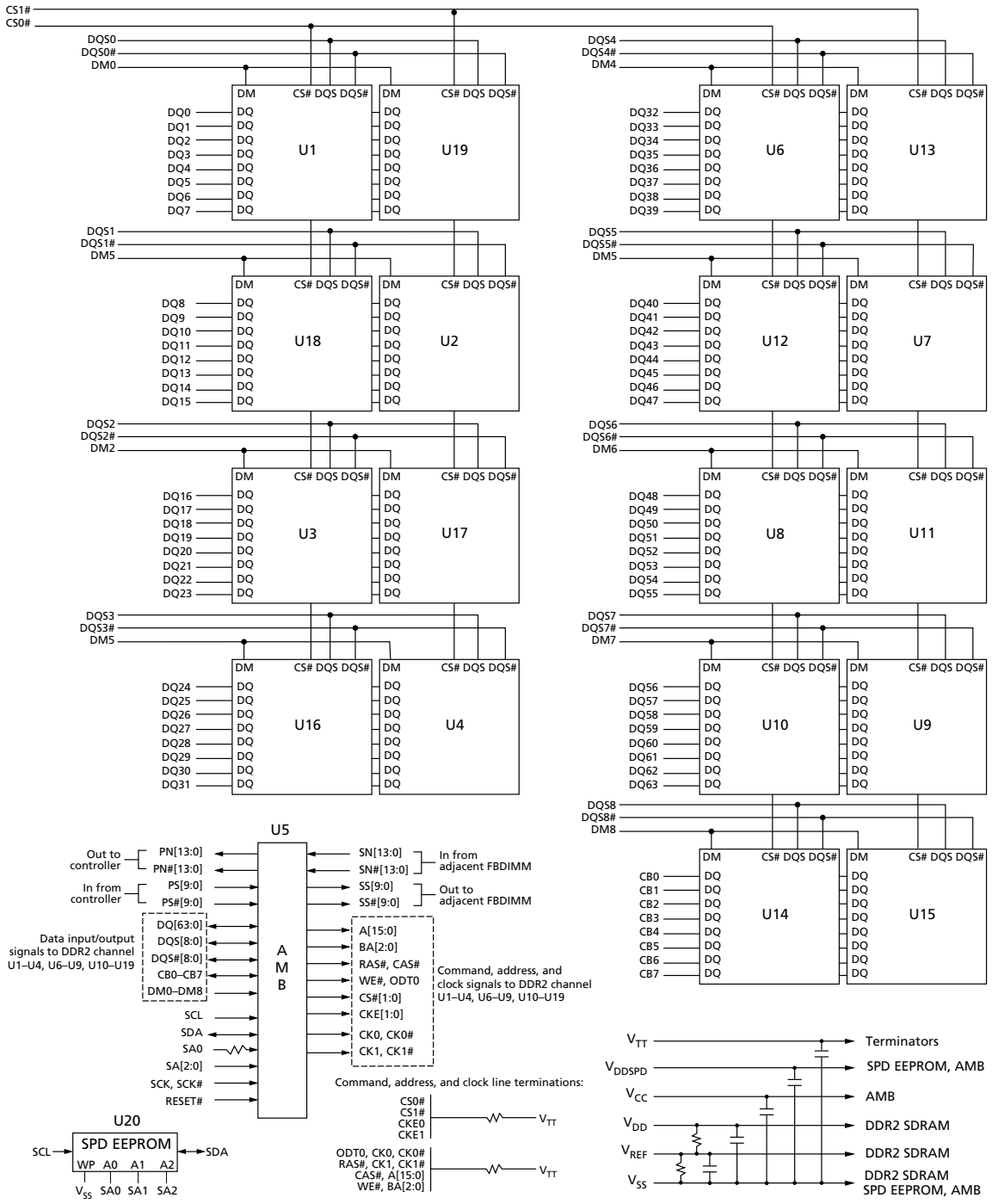
Functional Block Diagram

Figure 2: Functional Block Diagram



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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Voltage on any signal pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.3	1.75	V	1
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	–0.3	1.75	V	
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.5	2.3	V	
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	–0.5	2.3	V	
DDR2 SDRAM device operating case temperature	T_C	0	95	°C	2, 3
AMB device operating case temperature		0	110	°C	

Notes:
1. V_{IN} should not be greater than V_{CC}.
2. T_C is specified at 95°C only when using 2X refresh timing (^tREFI = 7.8µs at or below 85°C; ^tREFI = 3.9µs above 85°C); DDR2 SDRAM component data sheet.
3. See applicable DDR2 SDRAM component data sheet for ^tREFI and extended mode register settings. The ^tREFI parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

Table 7: Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	V_{CC}	1.455	1.50	1.575	V	
DDR2 SDRAM supply voltage	V_{DD}	1.5	1.55	1.9	V	
Termination voltage	V_{TT}	0.48 × V_{DD}	0.50 × V_{DD}	0.52 × V_{DD}	V	
EEPROM supply voltage	V_{DDSPD}	3.0	–	3.6	V	1
SPD input high (logic 1) voltage	$V_{IH(DC)}$	2.1	–	V_{DDSPD}	V	2
SPD input low (logic 0) voltage	$V_{IL(DC)}$	–0.6	–	0.8	V	2
RESET input high (logic 1) voltage	$V_{IH(DC)}$	1.0	–	–	V	3
RESET input low (logic 0) voltage	$V_{IL(DC)}$	–	–	0.5	V	2
Leakage current (RESET)	I_L	–90	–	90	µA	3
Leakage current (link)	I_L	–5	–	5	µA	4

Notes:
1. Applies to AMB and SPD.
2. Applies to SMBus and SPD bus signals.
3. Applies to AMB CMOS signal RESET#.
4. For all other AMB related DC parameters, refer to the high-speed differential link interface specification.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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IDD Specifications and Conditions

Table 8: I_{DD} Conditions

Symbol	Condition
$I_{DD_IDLE_0}$	**Idle current, single, or last DIMM:** L0 state; Idle (0% bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
$I_{DD_IDLE_1}$	**Idle current, first DIMM:** L0 state; Idle (0% bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
$I_{DD_ACTIVE_1}$	**Active power:** L0 state; 50% DRAM bandwidth; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH
$I_{DD_ACTIVE_2}$	**Active power, data pass through:** L0 state; 50% DRAM bandwidth to downstream DIMM; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable
$I_{DD_TRAINING}$	**Training:** Primary and secondary channels enabled; 100% toggle on all channel lanes; DRAMs idle; 0% bandwidth; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I_{DD_IBIST}	**IBIST over all IBIST modes:** DRAM idle (0% bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
I_{DD_EI}	**Electrical idle:** DRAM idle (0% bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW

Note: 1. Actual test conditions may vary from published JEDEC test conditions.

Table 9: I_{DD} Specifications – 2GB DDR2-667

Symbol	$I_{DD_IDLE_0}$	$I_{DD_IDLE_1}$	$I_{DD_ACTIVE_1}$	$I_{DD_ACTIVE_2}$	$I_{DD_TRAINING}$	I_{DD_IBIST}	I_{DD_EI}	Units
I_{CC}	2600	3400	3900	3700	4000	4500	2500	A
I_{DD}	1150	1150	2178	1150	1150	1150	326	A
Total power	6.3	7.5	10.3	8	8.5	9.3	4.6	W

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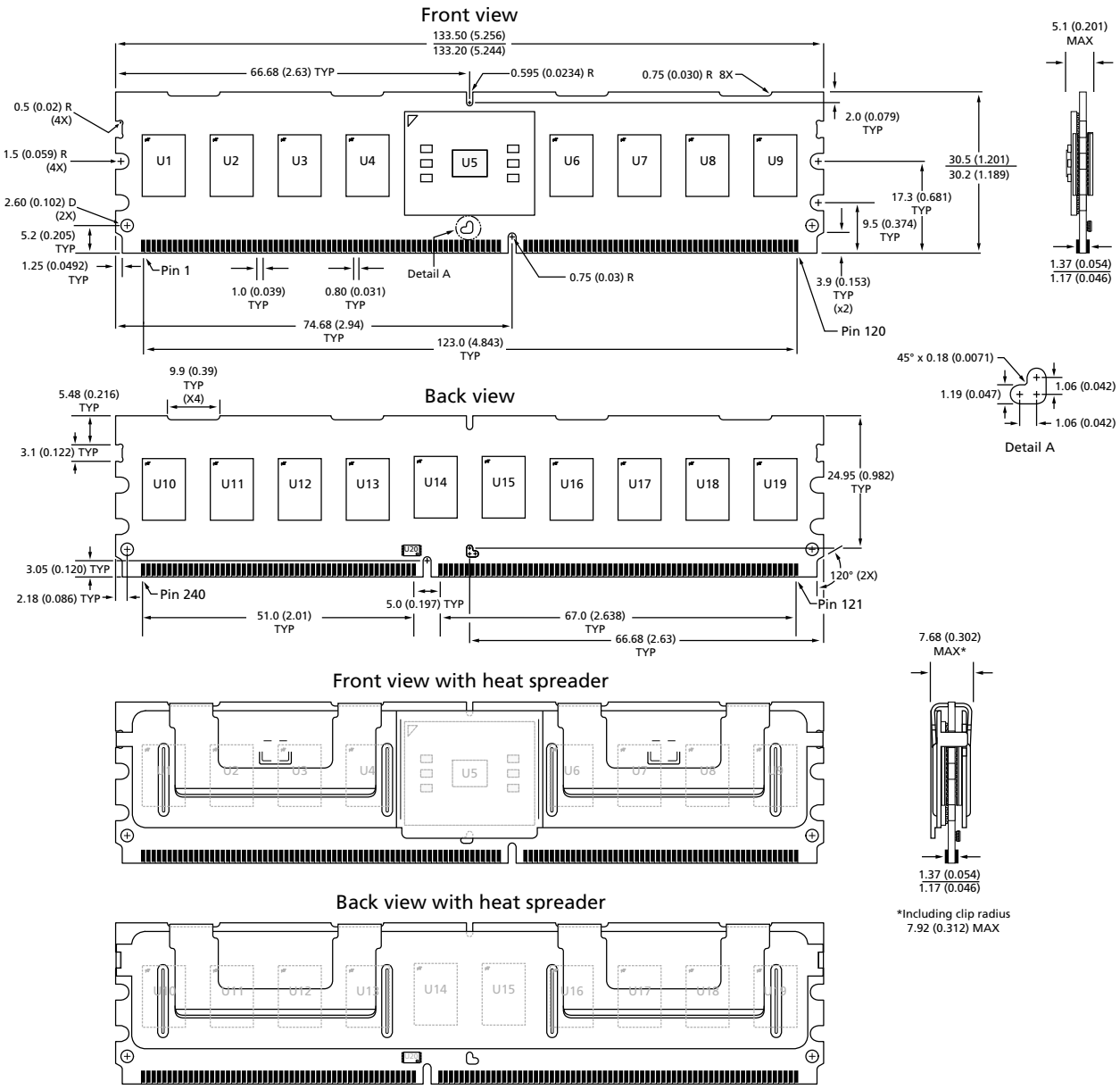
Module Dimensions

Figure 3: 240-Pin DDR2 FBDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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