MMDPE56G8DXP-0VB
MMCRE28G8MXP-0VB
MMCRE64G8MXP-0VB

PM800 - 1.8" SATA 3.0Gb/s MLC SSD

(NAND based Solid State Drive)

datasheet

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Table Of Contents

1.0 General Description 5
2.0 Mechanical Specification 6
2.1 Physical dimensions and Weight 6
3.0 Product Specifications 7
3.1 System Interface and Configuration 7
3.2 System Performance 7
3.3 Drive Capacity 7
3.4 Supply Voltage 7
3.5 System Power Consumption 7
3.6 System Reliability 7
3.7 Environmental Specifications 8
4.0 Electrical Interface Specification 8
4.1 Serial ATA Interface connector 8
4.2 Pin Assignments 9
5.0 Frame Information Structure (FIS) 10
5.1 Register - Host to Device 10
5.2 Register - Device to Host 11
5.3 Data 12
5.4 PIO Setup 12
5.5 DMA Activate - Device to Host 13
5.6 DMA Setup 13
5.7 Set Device Bits - Device to Host 13
6.0 Shadow Register Block registers Description 14
6.1 Command Register 14
6.2 Device Control Register 14
6.2.1 Field / bit description 14
6.3 Device / Head Register 14
6.3.1 Field / bit description 14
6.4 Error Register 14
6.4.1 Field / bit description 14
6.5 Features Register 15
6.6 Cylinder High (LBA High) Register 15
6.7 Cylinder Low (LBA Mid) Register 15
6.8 Sector Number (LBA low) Register 15
6.9 Sector Count Register 15
6.10 Status Register 15
6.10.1 Field / bit description 15
7.0 Command Descriptions 16
7.1 Supported ATA Commands 16
7.2 SECURITY FEATURE Set 16
7.2.1 SECURITY mode default setting 16
7.2.2 Initial setting of the user password 17
7.2.3 SECURITY mode operation from power-on 17
7.2.4 Password lost 17
7.3 SMART FEATURE Set (B0h) 17
7.3.1 Sub Command 17
7.3.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h) 17
7.3.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h) 17
7.3.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h) 18
7.3.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h) 18
7.3.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h) 18
7.3.1.6 S.M.A.R.T. Selective self-test routine 19
7.3.1.7 S.M.A.R.T. Read Log Sector (subcommand D5h) 20
7.3.1.8 S.M.A.R.T. Write Log Sector (subcommand D6h) 20
7.3.1.9 S.M.A.R.T. Enable Operations (subcommand D8h) 20
7.3.1.10 S.M.A.R.T. Disable Operations (subcommand D9h) 20
7.3.1.11 S.M.A.R.T. Return Status (subcommand DAh) 21
7.3.1.12 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh) 21

7.3.2 Device Attribute Data Structure 21
7.3.2.1 Data Structure Revision Number 22
7.3.2.2 Individual Attribute Data Structure 22
7.3.2.3 Off-Line Data Collection Status 23
7.3.2.4 Self-test execution status 23
7.3.2.5 Total time in seconds to complete off-line data collection activity 23
7.3.2.6 Current segment pointer 23
7.3.2.7 Off-line data collection capability 23
7.3.2.8 S.M.A.R.T. Capability 24
7.3.2.9 Error logging capability 24
7.3.2.10 Self-test failure check point 24
7.3.2.11 Self-test completion time 24
7.3.2.12 Data Structure Checksum 24
7.3.3 Device Attribute Thresholds data structure 24
7.3.3.1 Data Structure Revision Number 24
7.3.3.2 Individual Thresholds Data Structure 25
7.3.3.3 Attribute ID Numbers 25
7.3.3.4 Attribute Threshold 25
7.3.3.5 Data Structure Checksum 25
7.3.4 S.M.A.R.T. Log Directory 25
7.3.5 S.M.A.R.T. error log sector 26
7.3.5.1 S.M.A.R.T. error log version 26
7.3.5.2 Error log pointer 26
7.3.5.3 Device error count 26
7.3.5.4 Error log data structure 26
7.3.5.5 Command data structure 27
7.3.5.6 Error data structure 27
7.3.6 Self-test log structure 28
7.3.7 Selective self-test log data structure 28
7.3.8 Error reporting 29

8.0 OOB signaling and Phy Power State 29
8.1 OOB signaling 29
8.1.1 OOB signal spacing 29
8.2 Phy Power State 30
8.2.1 COMRESET sequence state diagram 30
8.2.2 Interface Power States 30
8.2.2.1 PHYRDY 30
8.2.2.2 Partial 30
8.2.2.3 Slumber 30
8.2.3 Partial/Slumber to PHYRDY 30
8.2.3.1 Host Initiated 30
8.2.3.2 Device Initiated 30
8.2.4 PHYRDY to Partial/Slumber 31
8.2.4.1 Host Initiated for Partial 31
8.2.4.2 Device Initiated for Partial 31

9.0 SATA II Optional Feature 32
9.1 Power Segment Pin P11 32
9.2 Activity LED indication 32
9.3 Asynchronous Signal Recovery 32

10.0 Identify Device Data 33

11.0 Ordering Information 35

12.0 Product Line up 35

1.0 General Description

The NSSD(Nand based Solid State Drive) of Samsung Electronics fully consists of semiconductor devices using NAND Flash Memory which provide high reliability and high performance for a storage media.
The NSSD doesn't have any moving parts such as platter(disk) and head media, which provides a better solution in a notebook PC and Tablet PC for a storage device providing higher performance, reduced latencies, and a low power consumption in a small form factor. The NSSD could also provide rugged features in industrial PC with an extreme environment with a high MTBF.
For easy adoption, the NSSD has the same host interface with Hard Disk Drives and has a same physical dimension.

•Density
- 256GB /128GB/64GB are available

•Form Factor
- 1.8" Type (54 x 78.5 x 5mm)

•Host interface
- Serial ATA interface of 3.0Gbps
- Fully complies with ATA/ATAPI-7 Standard (Partially Complies with ATA/ATAPI-8)
- Power Saving Modes: HIPM, DIPM (Partial / Slumber mode)
- Support NCQ : Up to 32 depth
- Synchronous Signal Recovery
- Activity LED indication (Pin7)

•Performance
- Host transfer rate: 300 MB/s
- Sequential Data Read : Up to 220 MB/s
- Sequential Data Write : Up to 175 MB/s (256GB)
  Up to 185 MB/s (128GB)
  Up to 120 MB/s (64GB)

* Actual performance may vary depending on use conditions and environment

•Power Consumption
- Active : 0.23 W (256GB)
  0.27 W (64/128GB)
- Idle/Standby/Sleep : 0.12 W (256GB)
  0.17 W (64/128GB)

* Active power is measured during excution of MobileMark* 2007.
* DIPM enabled

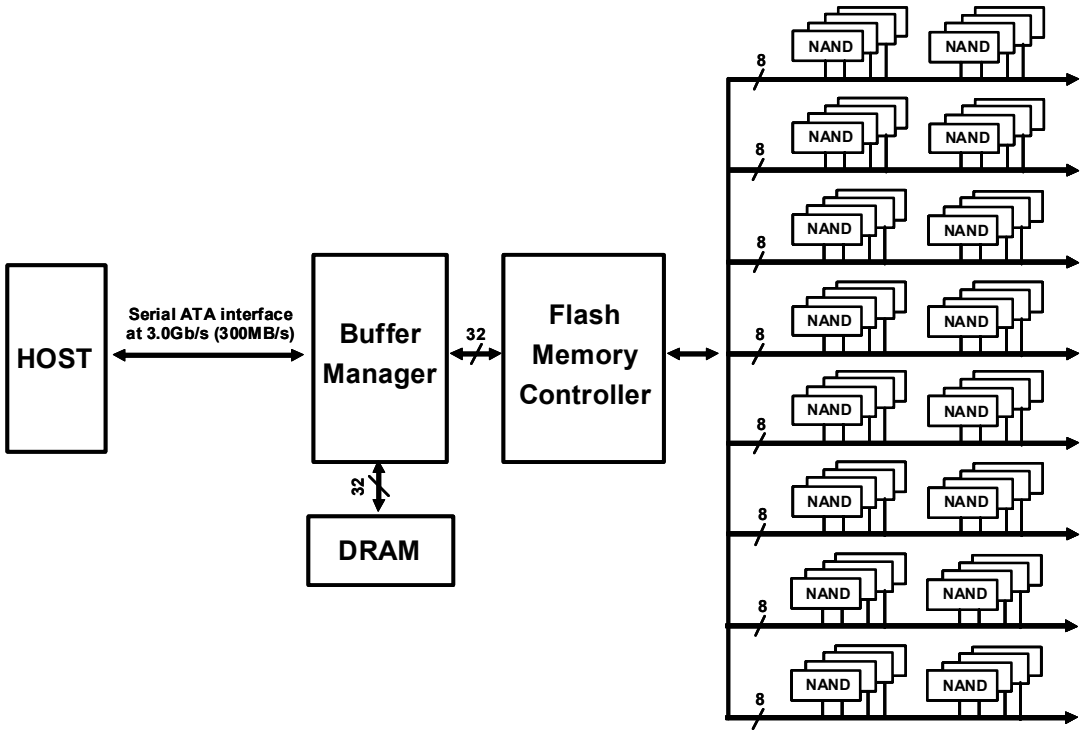
•Temperature
- Operating : 0°C to 70°C

•Shock
- Operating : 1500G, duration 0.5ms, Half Sine Wave
- Vibration : 20G Peak, 10~2000Hz,(15mins/Axis)x3 Axis

•MTBF
- 1,000,000 Hours

•Weight
- 256GB : 42g
- 128GB : 42g
- 64GB : 37g

•NSSD Functional Block Diagram

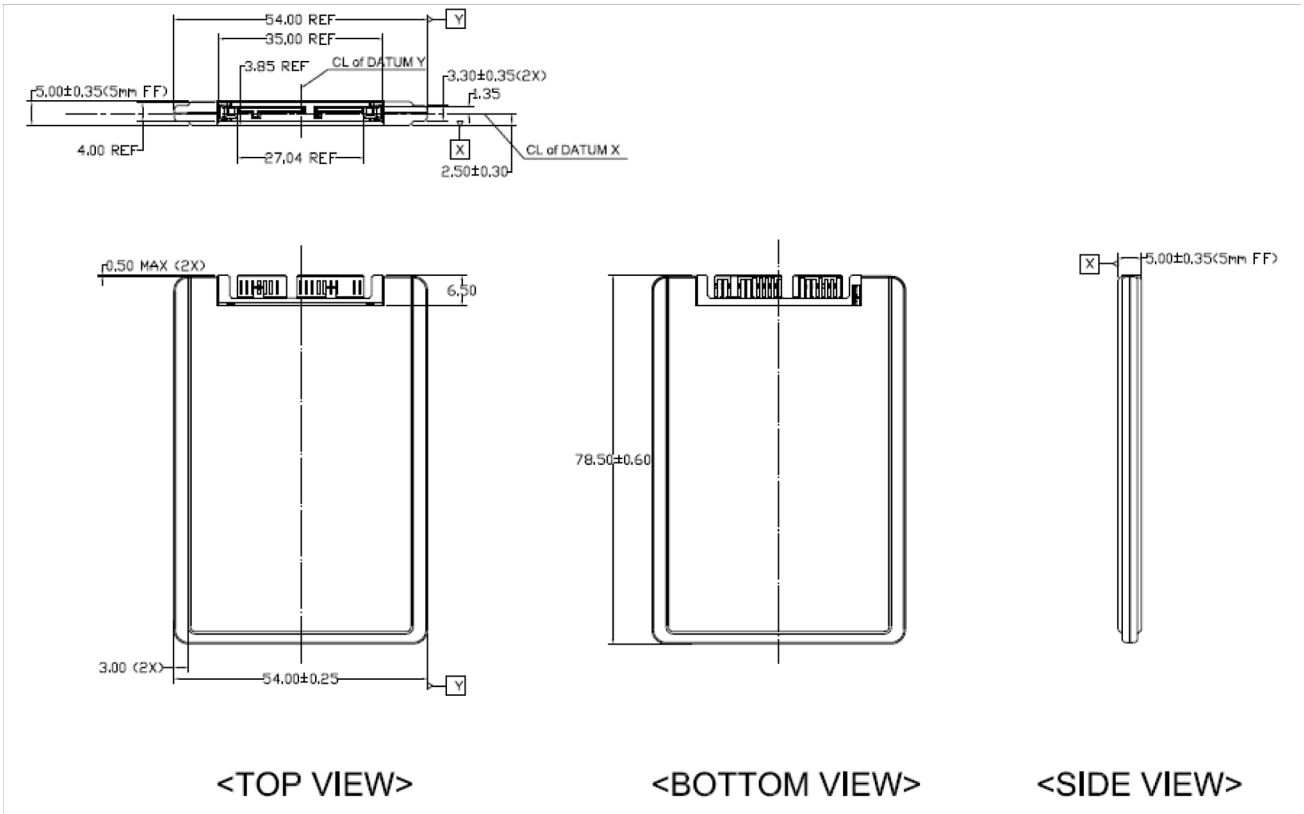


2.0 Mechanical Specification

2.1 Physical dimensions and Weight

Physical dimensions and Weight

Model	Height (mm)	Width (mm)	Length (mm)	Weigth (gram)
256GB	5.0 ± 0.35	54.0 ± 0.25	78.5 ± 0.6	42g
128GB	5.0 ± 0.35	54.0 ± 0.25	78.5 ± 0.6	42g
64GB	5.0 ± 0.35	54.0 ± 0.25	78.5 ± 0.6	37g



[Figure 2-1] Physical dimension

3.0 Product Specifications

3.1 System Interface and Configuration

- Burst read/write rate is 300 MB/sec (3.0 Gb/sec).
- Fully compatible with ATA-7 Standard
  (Partially Complies with ATA/ATAPI-8)

3.2 System Performance

Read / Write	MMCRE64G8MXP-0VB	MMCRE28G8MXP-0VB	MMDPE56G8DXP-0VB
Sequential Read Sector	Up to 220 MB/s	Up to 220 MB/s	Up to 220 MB/s
Sequential Write Sector	Up to 120 MB/s	Up to 185 MB/s	Up to 175 MB/s

* Actual performance may vary depending on use conditions and environment

3.3 Drive Capacity

	MMCRE64G8MXP-0VB	MMCRE28G8MXP-0VB	MMDPE56G8DXP-0VB
Unformatted Capacity	64GB	128 GB	256 GB
User-Addressable Sectors	125,045,424	250,069,680	500,118,192
Bytes per Sector	512 Bytes		

NOTE :
1 Megabyte (MB) = 1 Million bytes; 1 Gigabyte (GB) = 1 Billion bytes
* Actual usable capacity may be less (due to formatting, partitioning, operating system, applications or otherwise)

3.4 Supply Voltage

Item	Requirements
Allowable voltage	3.3V ± 5%
Allowable noise/ripple	100mV p-p or less

3.5 System Power Consumption

(Active power is measured during execution of MobileMark 2007, DIPM enabled)

Typical(W)	MMCRE64G8MXP-0VB	MMCRE28G8MXP-0VB	MMDPE56G8DXP-0VB
Active	0.27 W	0.27 W	0.23 W
Idle	0.17 W	0.17 W	0.12 W

3.6 System Reliability

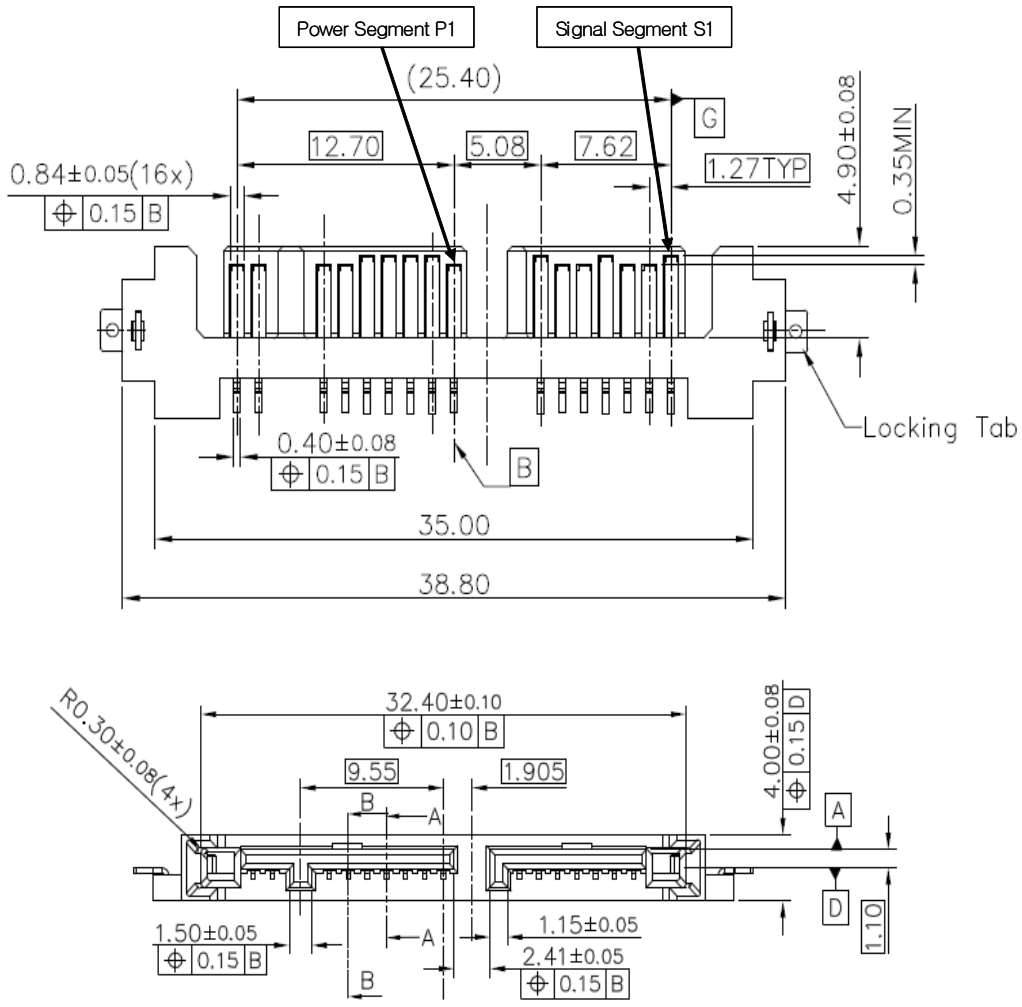
MTBF	1,000,000 Hours

3.7 Environmental Specifications

Features	Operating	Non-Operating
Temperature	0°C to 70°C	-55°C to 95°C
Humidity	5% to 95%, non-condensing	
Vibration	20G Peak, 10~2000Hz,(15mins/Axis)x3 Axis	
Shock	1500G, duration 0.5ms, Half Sine Wave	

4.0 Electrical Interface Specification

4.1 Serial ATA Interface connector



4.2 Pin Assignments

	No.	Plug Connector pin definition	
Signal	S1	GND	2nd mate
	S2	A+	Differential signal A from Phy
	S3	A-	
	S4	GND	2nd mate
	S5	B-	Differential signal B from Phy
	S6	B+	
	S7	GND	2nd mate
Key and spacing spearate signal and power segments			
Power	P1	V33	3.3V power, 2nd mate
	P2	V33	3.3V power, Pre-charge, 1st mate
	P3	GND	1st mate
	P4	GND	1st mate
	P5	V5	5V Power, Pre-charge (Unused), 1st mate
	P6	V5	5V Power, (Unused), 2nd mate
	P7	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
	Key	Key	Key
	P8	Optional	Vendor specific, 2nd mate
	P9	Optional	Vendor specific, 2nd mate

NOTE :
Uses 3.3V power only, 5V and 12V power are not used.

5.0 Frame Information Structure (FIS)

5.1 Register - Host to Device

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	Features	Command	C R R Reserved (0)	FIS Type (27h)
1	Device	LBA High	LBA Mid	LBA Low
2	Features (exp)	LBA High (exp)	LBA Mid (exp)	LBA Low (exp)
3	Control	Reserved (0)	Sector Count (exp)	Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)	Reserved (0)

[Table 5-1] Register - Host to Device layout (48bit LBA mode, EXT commands, NCQ commands)

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	Features	Command	C R R Reserved (0)	FIS Type (27h)
1	Device/Head	Cylinder High	Cylinder Low	Sector Number
2	Reserved (0)	Reserved (0)	Reserved (0)	Reserved (0)
3	Control	Reserved (0)	Reserved (0)	Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)	Reserved (0)

[Table 5-2] Register - Host to Device layout (CHS mode)

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	Features	Command	C R R Reserved (0)	FIS Type (27h)
1	Device/LBA 27:24	LBA 23:16	LBA 15:8	LBA 7:0
2	Reserved (0)	Reserved (0)	Reserved (0)	Reserved (0)
3	Control	Reserved (0)	Reserved (0)	Sector Count
4	Reserved (0)	Reserved (0)	Reserved (0)	Reserved (0)

[Table 5-3] Register - Host to Device layout (28bit LBA mode)

5.2 Register - Device to Host

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	S	Reserved (0)							FIS Type (34h)						
1	Device								LBA High								LBA Mid										LBA Low						
2	Features (exp)								LBA High (exp)								LBA Mid (exp)										LBA Low (exp)						
3	Reserved (0)								Reserved (0)								Sector Count (exp)										Sector Count						
4	Reserved (0)								Reserved (0)								Reserved (0)										Reserved (0)						

[Table 5-4] Register - Device to Host layout (48bit LBA mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	S	Reserved (0)							FIS Type (34h)						
1	Device/Head								Cylinder High								Cylinder Low										Sector Number						
2	Reserved (0)								Reserved (0)								Reserved (0)										Reserved (0)						
3	Reserved (0)								Reserved (0)								Reserved (0)										Sector Count						
4	Reserved (0)								Reserved (0)								Reserved (0)										Reserved (0)						

[Table 5-5] Register - Device to Host layout (CHS mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	S	Reserved (0)							FIS Type (34h)						
1	Device/LBA 27:24								LBA 23:16								LBA 15:8										LBA 7:0						
2	Reserved (0)								Reserved (0)								Reserved (0)										Reserved (0)						
3	Reserved (0)								Reserved (0)								Reserved (0)										Sector Count						
4	Reserved (0)								Reserved (0)								Reserved (0)										Reserved (0)						

[Table 5-6] Register - Device to Host layout (28bit LBA mode)

5.3 Data

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11 10	9 8 7 6 5 4 3 2 1 0
0	Reserved (0)	Reserved (0)	R	R	R	Reserved (0)	FIS Type (48h)
...							
...	N DWORDs of data (minimum of DWORD - maximum of 2048 DWORDs						
n							

[Table 5-7] Register - Data FIS layout

5.4 PIO Setup

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11 10	9 8 7 6 5 4 3 2 1 0
0	Error	Status	R	I	S	Reserved (0)	FIS Type (34h)
1	Device	LBA High	LBA Mid				LBA Low
2	Reserved (0)	LBA High (exp)	LBA Mid (exp)				LBA Low (exp)
3	E_ STATUS	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Transfer Count				

[Table 5-8] Register - PIO Setup layout (48bit LBA mode: Read/Write Sector EXT)

	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12 11 10	9 8 7 6 5 4 3 2 1 0
0	Error	Status	R	I	S	Reserved (0)	FIS Type (34h)
1	Device/Head	Cylinder High	Cylinder Low				Sector Number
2	Reserved (0)	Reserved (0)	Reserved (0)				Reserved (0)
3	E_ STATUS	Reserved (0)	Sector Count (exp)				Sector Count
4	Reserved (0)	Reserved (0)	Transfer Count				

[Table 5-9] PIO Set up layout (CHS mode: Commands include PIO data transfer)

5.5 DMA Activate - Device to Host

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Reserved (0)								R	R	R	Reserved (0)					FIS Type (39h)							

[Table 5-10] DMA Activate Layout (Write DMA/Write DMA Queued/Service)

5.6 DMA Setup

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Reserved (0)								A	I	D	Reserved (0)					FIS Type (A1h)							
1	0																													TAG		
2	0																															
3	Reserved (0)																															
4	DMA Buffer Offset																															
5	DMA Transfer Count																															
6	Reserved (0)																															

[Table 5-11] DMA Setup layout (NCQ, Read/Write FpDMA Queued)

5.7 Set Device Bits - Device to Host

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								R	Status Hi			R	Status Lo			N	I	R	Reserved (0)					FIS Type (A1h)							
1	SActive 31:0																															

[Table 5-12] Set Device Bits layout (NCQ, Result of Read/Write FpDMA Queued commands)

6.0 Shadow Register Block registers Description

6.1 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register.

6.2 Device Control Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register.

6.2.1 Field / bit description

7	6	5	4	3	2	1	0
HOB	-	-	-	-	SRST	nIEN	0

• HOB is defined by the 48bit Address feature set. A write to any Command register shall clear the HOB bit to zero.
• SRST is the host software reset bit. SRST=1 indicates that the drive is held reset and sets BSY bit in Status register. Setting SRST=0 re-enables the device.
• nIEN is the enable bit for the device Assertion of INTRQ to the host. When nIEN=0, and the device is selected by Drice select bit in DEVICE/HEAD register, device interrupt to the host is enabled. When this bit is set, the "I' bit in the Register Host to Device, PIO setup, Set Device Bits and DMA Set Up will be set, whether pending interrup is found or not.

6.3 Device / Head Register

6.3.1 Field / bit description

The content of this register shall take effect when written.

7	6	5	4	3	2	1	0
-	L	-	DEV	HS3	HS2	HS1	HS0

• L : Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
• DEV: Device select. Cleared to zero selects Device 0. Set to one selects Device1.
• HS3, HS2, HS1, HS0 : Head select bits. The HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

6.4 Error Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. All other registers required for the command must be set up before writing the Command Register.

6.4.1 Field / bit description

7	6	5	4	3	2	1	0
ICRC	UNC	0	IDNF	0	ABRT	TKONF	AMNF

• ICRC: Interface CRC Error. CRC=1 indicates a CRC error has occurred on the data bus during a Ultra-DMA transfer.
• UNC: Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.
• IDNF: ID Not Found. IDN=1 indicates the requested sector's ID field cound not be found .
• ABRT: Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.
• TKONF: Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.
• AMNF: Address Mark Not Found. When AMN=1, it indicates that the data address mark has not been found after finding the correct ID field for the requested sector.

6.5 Features Register

This register is command specific. This is used with the Set Features command, S.M.A.R.T. Function Set command.

6.6 Cylinder High (LBA High) Register

This register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

6.7 Cylinder Low (LBA Mid) Register

This register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.
When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15, and the "previous content" contains Bits 32-39

6.8 Sector Number (LBA low) Register

This register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.
When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7, and the "previous content" contains Bits 24-31.

6.9 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified.
If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.
The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

6.10 Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.
If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.
If BSY=1, no other bits in the register are valid. And read/write operations of any other register are negated in order to avoid the returning of the contesnts of this register instead of the other registers' contents.

6.10.1 Field / bit description

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

• BSY : Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

• DRDY : Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command.

• DF : Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is read by the host.

• DSC : Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the
host, at which time the bit again indicates the current seek complete status.
When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.

• DRQ : Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

• CORR : Corrected Data. Always 0.

• IDX : Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revoltion, the host may not see it set to
1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.

• ERR : ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

7.0 Command Descriptions

7.1 Supported ATA Commands

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
CHECK POWER MODE	E5h, 98h	SEEK	70h
DEVICE CONFIGURATION FREEZE LOCK	B1h/C1h	SET FEATURES	EFh
DEVICE CONFIGURATION IDENTIFY	B1h/C2h	SET MAX ADDRESS	F9h/00h
DEVICE CONFIGURATION RESTORE	B1h/C0h	SET MAX ADDRESS EXT	37h
DEVICE CONFIGURATION SET	B1h/C3h	SET MAX FREEZE LOCK	F9h/04h
DOWNLOAD MICROCODE	92h	SET MAX LOCK	F9h/02h
EXECUTE DEVICE DIAGNOSTIC	90h	SET MAX SET PASSWORD	F9h/01h
FLUSH CACHE	E7h	SET MAX UNLOCK	F9h/03h
FLUSH CACHE EXT	EAh	SET MULTIPLE MODE	C6h
IDENTIFY DEVICE	ECh	SLEEP	E6h, 99h
IDLE	E3h, 97h	SMART DISABLE OPERATIONS	B0h/D9h
IDLE IMMEDIATE	E1h, 95h	SMART ENABLE OPERATIONS	B0h/D8h
INITIALIZE DEVICE PARAMETERS	91h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	B0h/D2h
READ BUFFER	E4h	Enable/Disable Auto-Offine	B0h/DBh
READ DMA EXT	25h	SMART EXECUTE OFF-LINE IMMEDIATE	B0h/D4h
READ DMA with Retry	C8h	SMART READ ATTRIBUTE THRESHOLDS	B0h/D1h
READ DMA without Retry	C9h	SMART READ DATA	B0h/D0h
READ LOG EXT	2Fh	SMART READ LOG	B0h/D5h
READ MULTIPLE	C4h	SMART RETURN STATUS	B0h/DAh
READ MULTIPLE EXT	29h	SMART SAVE ATTRIBUTE VALUES	B0h/D3h
READ NATIVE MAX ADDRESS	F8h	SMART WRITE LOG	B0h/D6h
READ NATIVE MAX ADDRESS EXT	27h	STANDBY	E2h, 96h
READ SECTORS EXT	24h	STANDBY IMMEDIATE	E0, 94
READ SECTORS with Retry	20h	WRITE BUFFER	E8
READ SECTORS without Retry	21h	WRITE DMA EXT	35
READ VERIFY SECTORS EXT	42h	WRITE DMA with Retry	CA
READ VERIFY SECTORS with Retry	40h	WRITE DMA without Retry	CB
READ VERIFY SECTORS without Retry	41h	WRITE LOG EXT	3F
SECURITY DISABLE PASSWORD	F6h	WRITE MULTIPLE	C5
SECURITY ERASE PREPARE	F3h	WRITE MULTIPLE EXT	39
SECURITY ERASE UNIT	F4h	WRITE SECTORS EXT	34
SECURITY FREEZE LOCK	F5h	WRITE SECTORS with Retry	30
SECURITY SET PASSWORD	F1h	WRITE SECTORS without Retry	31
SECURITY UNLOCK	F2h		

7.2 SECURITY FEATURE Set

The Security mode features allow the host to implement a securtity password system to prevent unauthorized access to the disk drive.

7.2.1 SECURITY mode default setting

The NSSD is shipped with master password set to 20h value(ASCII blanks) and the lock function disabled.
The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enableing the lock function.

7.2.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on

7.2.3 SECURITY mode operation from power-on

In locked mode, the NSSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

7.2.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data.
However, the drive can be unlocked using the master password.

If the user password is lost and Maxium security level is set, it is impossible to access data.
However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

7.3 SMART FEATURE Set (B0h)

The SMART Feature Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The SMART Feature Set command has several separate subcommands which are selectable via the device's Features Register when the SMART Feature Set command is issued by the host. In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Feature Set command.

7.3.1 Sub Command

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Subcommand	Code	Subcommand	Code
SMART READ DATA	D0h	SMART WRITE LOG	D6h
SMART READ ATTRIBUTE THRESHOLDS	D1h	SMART ENABLE OPERATIONS	D8h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h	SMART DISABLE OPERATIONS	D9h
SMART SAVE ATTRIBUTE VALUES	D3h	SMART RETURN STATUS	DAh
SMART EXECUTE OFF-LINE IMMIDIATE	D4h	SMART ENABLE/ DISABLE AUTOMATIC OFF-LINE	DBh
SMART READ LOG	D5h		

7.3.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated Attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

7.3.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the S.M.A.R.T. Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device.

7.3.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)

This subcommand enables and disables the attribute auto save feature of the device. The S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector at the timing of the first transition to Active idle mode and after 15 minutes after the last saving of Attribute Values. This subcommand causes the auto save feature to be disabled. The state of the Attribute Autosave feature—either enabled or disabled—will be preserved by the device across the power cycle.
A value of 00h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or a power-down.
A value of F1h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be enabled. Any other nonzero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will not change the current Autosave status. The device will respond with the error code specified in Table 7-9: “S.M.A.R.T. Error Codes” on page 30.
The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations.
Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

7.3.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

7.3.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an offline mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The LBA Low register shall be set to specify the operation to be executed.

LBA Low	Subcommand
00h	Execute S.M.A.R.T. off-line data collection routine immediately
01h	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
02h	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute S.M.A.R.T. Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute S.M.A.R.T. short self-test routine immediately in captive mode
82h	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode
84h	Execute S.M.A.R.T. selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

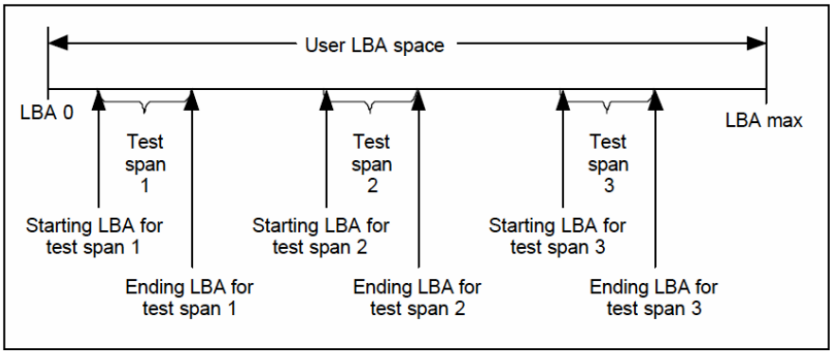
Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (see Table 7-1: “Device Attribute Data Structure” on page 23) and ATA registers and then executes the command completion. See definitions below.

Status Set ERR to one when the self-test has failed
Error Set ABRT to one when the self-test has failed
LBA Low Set to F4h when the self-test has failed
LBA High Set to 2Ch when the self-test has failed

7.3.1.6 S.M.A.R.T. Selective self-test routine

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This selftest routine shall include the initial tests performed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress.

The user may choose to do read scan only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Figure on page 21 shows an example of a Selective selftest definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.



After the scan of the selected spans described above, a user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the device shall then set the offline scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall completed as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the device is powered-down before the off-line scan is completed, the off-line scan shall resume when the device is again powered up. From power-up, the resumption of the scan shall be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion.

During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log.

A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log (see 7.3.7). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

7.3.1.7 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the indicated log sector contents to the host. Sector count sepcifies the number of sectors to be read from the specified log. The log transfferred by the drive shall start at the first sector in the speicified log, regardless of the sector count requested. Sector nubmer indicates the log sector to be returned as described in the following Table.

Log sector address	Content	
00h	Log directory	RO
01h	SMART error log	RO
02h	Comprehensive SMART error log	RO
04h-05h	Reserved	RO
06h	SMART self-test log	RO
08h	Reserved	RO
09h	Selective self-test log	RW
0Ah-7Fh	Reserved	RO
80h-9Fh	Host vendor specific	R/W
A0h-FFh	Reserved	VS

RO - Log is read only by the host.
R/W - Log is read or written by the host.
VS - Log is vendor specific thus read/write ability is vendor specific.

7.3.1.8 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. The 512 bytes of data are transferred at a command and the LBA Low value shall be set to one. The LBA Low shall be set to specify the log sector address. If a Rea Only log sector is specified, the device returns ABRT error.

7.3.1.9 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values. Upon receipt of the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

7.3.1.10 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute auto save feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.

Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled, and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand—returning the error code as specified in Table 7-9: “S.M.A.R.T. Error Codes” on page 30.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command.

7.3.1.11 S.M.A.R.T. Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the S.M.A.R.T. Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the LBA Mid register, C2h into the LBA High register, clears BSY, and asserts INTRQ.

If the device detects a Threshold Exceeded Condition for prefailure attributes, the device loads F4h into the LBA Mid register, 2Ch into the LBA High register, clears BSY, and asserts INTRQ. Advisory attributes never result in a negative reliability condition.

7.3.1.12 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities.

The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count	Feature Description
00h	Disable Automatic Off-line
F8h	Enable Automatic Off-line

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence.

A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled.

Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in Table 7-9: “S.M.A.R.T. Error Codes” on page 30.

7.3.2 Device Attribute Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand.

Byte	Descriptions
0~1	Data structure revision number
2~361	1st - 30th Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374-510	Reserved
511	Data structure checksum

[Table 7-1] Device Attribute Data Structure

7.3.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

7.3.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Byte	Descriptions
0	Attribute ID number 01-FFh
1~2	Status flag bit 0 (pre-failure/advisory bit) bit 0 = 0 : If attribute value is less than the threshold, the drive is in advisory condtion. Product life period may expired. bit 0 = 1 : If attribut value is less than the threshold, the drive is in pre-failure condition. The drive may have failure. bit 1 (on-line data collection bit) bit 1 = 0 : Attribute value will be changed during off-line data collection operation. bit 1 = 1 : Attribute value will be changed during normal operation. bit 2 (Performance Attribute bit) bit 3 (Error rate Attribute bit) bit 4 (Event Count Attribute bit) bit 5 (Self-Preserving Attribute bit) bit 6-15 Reserved
3	Attribute value 01h-FDh *1 00h, FEh, FFh = Not in use 01h = Minimum value 64h = Initial value Fdh = Maximum value
4	Worst Ever normalized Attribute Value (valid values from 01h-FEh)
5~10	Raw Attribute Value Attribute specific raw data (FFFFFFh - reserved as saturated value)
11	Reserved (00h)
*1 For ID = 199 CRC Error Count	

Attribute ID Numbers: Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers. The names marked with (*) indicate that the corresponding Attribute Values is fixed value for compatibility.

ID	Attribute Name
9	Power-on Hours
12	Power-on Count
178	Used Reserved Block Count(Chip)
179	Used Reserved Block Count(Total)
180	Unused Reserved Block Count(Total)
183	Runtime bad blk (total)

7.3.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7 Automatic Off-line Data Collection Status
0 Automatic Off-line Data Collection is disabled.
1 Automatic Off-line Data Collection is enabled.

Bits 0–6 represent a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started.
2	All segments completed without errors. In this case the current segment pointer is equal to the total segments required.
3	Off-line activity in progress.
4	Off-line data collection is suspended by the interrupting command.
5	Off-line data collecting is aborted by the interrupting command.
6	Off-line data collection is aborted with a fatal error.

7.3.2.4 Self-test execution status

Bit	Definition
0-3	Percent Self-test remaining. An approximation of the percent of the self-test routine remaining until completion given in ten percent increments. Valid values are 0 through 9.
4-7	Current Self-test execution status.
0	The self-test routine completed without error or has never been run.
1	The self-test routine was aborted by the host.
2	The self-test routine was interrupted by the host with a hard or soft reset.
3	The device was unable to complete the self-test routine due to a fatal error or unknown test error.
4	The self-test routine was completed with an unknown element failure.
5	The self-test routine was completed with an electrical element failure.
6	The self-test routine was completed with a servo element failure.
7	The self-test routine was completed with a read element failure.
15	The self-test routine is in progress.

7.3.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

7.3.2.6 Current segment pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1, 01h is always returned in this field.

7.3.2.7 Off-line data collection capability

Bit	Definition
0	Execute Off-line Immediate implemented bit
	0 S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented
	1 S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/disable Automatic Off-line implemented bit
	0 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented
	1 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented
2	Abort/restart off-line by host bit
	0 The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
	1 The device will abort off-line data collection activity upon receipt of a new command Bit Definition
3	Off-line Read Scanning implemented bit
	0 The device does not support Off-line Read Scanning
	1 The device supports Off-line Read Scanning
4	Self-test implemented bit
	0 Self-test routing is not implemented
	1 Self-test routine is implemented
5	Reserved (0)
6	Selective self-test routine is not implemented
	0 Selective self-test routine is not implemented
	1 Selective self-test routine is implemented
7	Reserved (0)

7.3.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute auto save capability. If bit = 1, the device supports the S.M.A.R.T. ENABLE/ DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

7.3.2.9 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit = 1, the device supports the Error Logging

7.3.2.10 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

7.3.2.11 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

7.3.2.12 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

7.3.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specification for byte ordering, that is, that the least significant byte occupies the lowest numbered byte address location in the field.
The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Byte	Descriptions
0~1	Data structure revision number
2~361	1st - 30th Individual attribute data
362 ~ 379	Reserved
380 ~ 510	Vendor specific
511	Data structure checksum

[Table 7-2] Device Attribute Thresholds Data Structure

7.3.3.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

7.3.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Byte	Descriptions
0	Attribute ID Number (01h to FFh)
1	Attribute Threshold (for comparison with Attribute Values from 00h to FFh) 00h - "always passing" threshold value to be used for code test purposes 01h - minimum value for normal operation FDh - maximum value for normal operation FEh - invalid for threshold value FFh - "always failing" threshold value to be used for code test purposes
2~11	Reserved (00h)

7.3.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

7.3.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use the "S.M.A.R.T. Write Attribute Threshold" sub-command to override these preset values in the Threshold sectors.

7.3.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

7.3.4 S.M.A.R.T. Log Directory

The following defines the 512 bytes that make up the S.M.A.R.T. Log Directory. The S.M.A.R.T. Log Directory is on S.M.A.R.T. Log Address zero and is defined as one sector long.

Byte	Descriptions
0~1	S.M.A.R.T. Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
...	
510	Number of sectors in the log at log address 255
511	Reserved

[Table 7-3] S.M.A.R.T. Log Directory

The value of the S.M.A.R.T. Logging Version word shall be 01h. The logs at log addresses 80-9Fh are defined as 16 sectors long.

7.3.5 S.M.A.R.T. error log sector

The following defines the 512 bytes that make up the S.M.A.R.T. error log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specifications for byte ordering.

Byte	Descriptions
0	S.M.A.R.T. error log version
1	Error log pointer
2-91	1st error log data structure
92-181	2nd error log data structure
182-271	3rd error log data structure
272-361	4th error log data structure
362-451	5th error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

[Table 7-4] S.M.A.R.T. error log sector

7.3.5.1 S.M.A.R.T. error log version

This value is set to 01h.

7.3.5.2 Error log pointer

This points to the most recent error log data structure. Only values 1 through 5 are valid.

7.3.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

7.3.5.4 Error log data structure

The data format of each error log structure is shown below.

Byte	Descriptions
n ~ n+11	1st command data structure
n+12 ~ n+23	2nd command data structure
n+24 ~ n+35	3rd command data structure
n+36 ~ n+47	4th command data structure
n+48 ~ n+59	5th command data structure
n+60 ~ n+89	Error data structure

[Table 7-5] Error log data structure

7.3.5.5 Command data structure

Data format of each command data structure is shown below.

Byte	Descriptions
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

[Table 7-6] Command data structure

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

7.3.5.6 Error data structure

Data format of error data structure is shown below.

Byte	Descriptions
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 - n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

[Table 7-7] Error data structure

Extended error information will be vendor specific.

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique

The value of x is vendor specific and may be different for each state.

7.3.6 Self-test log structure

The following defines the 512 bytes that make up the Self-test log sector.

Byte	Byte
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
...	...
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

[Table 7-8] Self-test log data structure

NOTE :
N is 0 through 20
The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

7.3.7 Selective self-test log data structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the specifications for byte ordering.

Byte	Description	Read/Write
0-1	Data structure revision	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4+	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags	R/W
504-507	Vendor Specific	Vendor specific
508-509	Selective self test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

7.3.8 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the LBA High and LBA Mid registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. Disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 04h
The device is unable to write to its Attribute Values data structure.	51h	10h or 40h

[Table 7-9] SMART Error Codes

8.0 OOB signaling and Phy Power State

8.1 OOB signaling

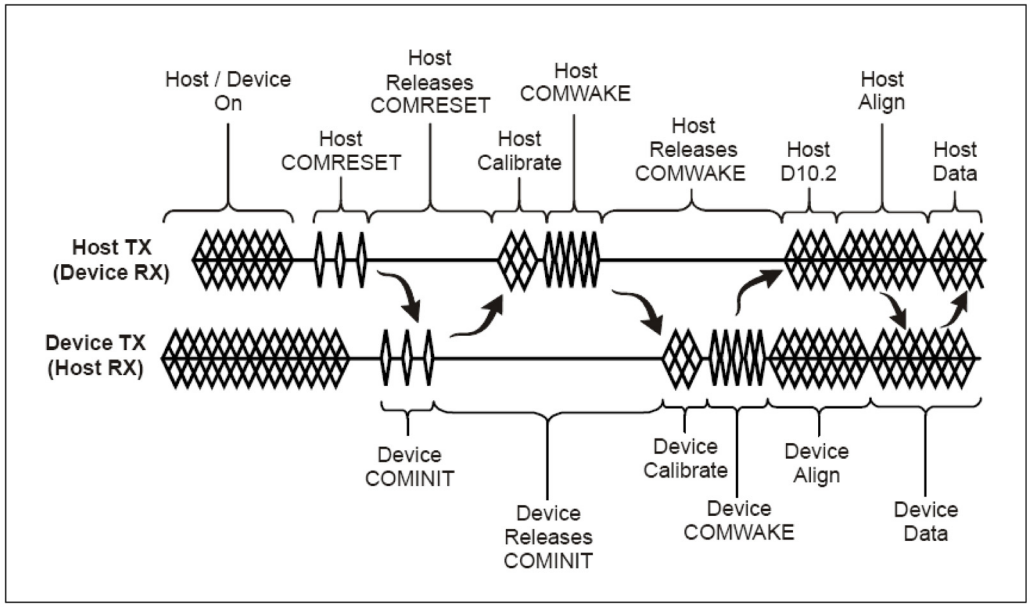
8.1.1 OOB signal spacing

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET,COMINIT, and COMWAKE. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in following Figure and Table. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (Partial or Slumber)

Time	Value
T1	106.7 ns
T2	320 ns

8.2 Phy Power State

8.2.1 COMRESET sequence state diagram



8.2.2 Interface Power States

8.2.2.1 PHYRDY

The Phy logic and main PLL are both on and active. The interface is synchronized and capable of receiving and sending data.

8.2.2.2 Partial

The Phy logic is powered, but is in a reduced power state. Both signal lines on the interface are at a neutral logic state (common mode voltage). The exit latency from this state shall be no longer than 10 us.

8.2.2.3 Slumber

The Phy logic is powered but is in a reduced power state. The exit latency from this state shall be no longer than 10 ms.

8.2.3 Partial/Slumber to PHYRDY

8.2.3.1 Host Initiated

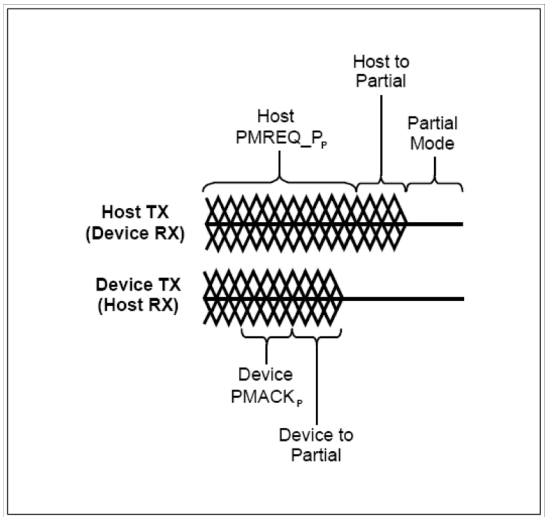
The host may initiate a wakeup from the Partial or Slumber states by entering the power-on sequence at the “Host COMWAKE” point in the state machine. Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGNP primitives at the speed determined at power-on.

8.2.3.2 Device Initiated

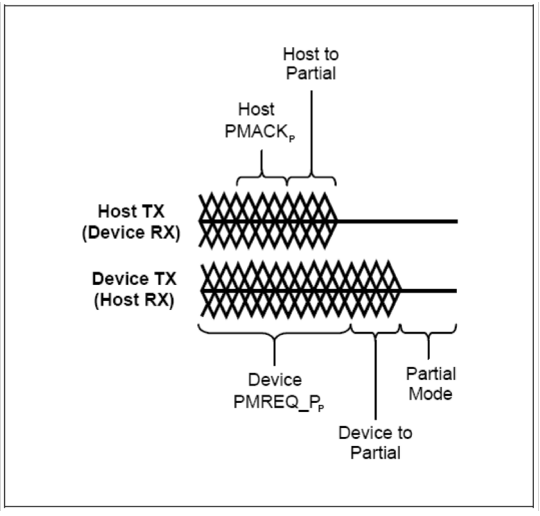
The device may initiate a wakeup from the Partial or Slumber states by entering the power-on sequence at the “Device COMWAKE” point in the state machine. Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGNP primitives at the speed determined at power-on.

8.2.4 PHYRDY to Partial/Slumber

8.2.4.1 Host Initiated for Partial



8.2.4.2 Device Initiated for Partial



*For Slumber, the same sequence applies except PMREQ_PP is replaced with PMREQ_SP and Partial is replaced with Slumber.

9.0 SATA II Optional Feature

9.1 Power Segment Pin P11

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication and it may be used by the host to indicate whether staggered spinup should be used. To accomplish both of these goals, pin P11 acts as an input from the host to the device prior to PHYRDY for staggered spin-up control and then acts as an output from the device to the host after PHYRDY for activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications.
A host may only support one pin P11 feature, either receiving activity indication or staggered spin-up disable control. If a host supports receiving activity indication via pin P11, then the host shall not use pin P11 to disable staggered spin-up. If a host does not support receiving activity indication via pin P11, then the host may use pin P11 to disable staggered spin-up.

9.2 Activity LED indication

The signal provides for activity indication is a low-voltage low-current driver intended for efficient integration into present and future IC manufacturing processes. The signal is NOT suitable for directly driving an LED and must first be buffered using a circuit external to the drive before driving an LED.

9.3 Asynchronous Signal Recovery

Phys may support asynchronous signal recovery for those applications where the usage model of device insertion into a receptacle does not apply. When signal is lost, both the host and the device may attempt to recover the signal. A host or device shall determine loss of signal as represented by a transition from PHYRDY to PHYRDYn, which is associated with entry into states LSI: NoCommErr or LS2:NoComm within the Link layer. Note that negation of PHYRDY does not always constitute a loss of signal. Recovery of the signal is associated with exit from state LS2:NoComm. If the device attempts to recover the signal before the host by issuing a COMINIT, the device shall return its signature following completion of the OOB sequence which included COMINIT. If a host supports asynchronous signal recovery, when the host receives an unsolicited COMINIT, the host shall issue a COMRESET to the device. When a COMRESET is sent to the device in response to an unsolicited COMINIT, the host shall set the Status register to 7Fh and shall set all other Shadow Command Block Registers to FFh. When the COMINIT is received in response to the COMRESET which is associated with entry into state HP2B:HR_AwaitNoCOMINIT, the Shadow Status register value shall be updated to either FFh or 80h to reflect that a device is attached.

10.0 Identify Device Data

Word	64GB	128GB	256GB	Description
0	0x0040	0x0040	0x0040	General information
1	0x3FFF	0x3FFF	0x3FFF	Number of logical cylinders
2	0xC837	0xC837	0xC837	Specific configuration
3	0x0010	0x0010	0x0010	Number of logical heads
4 - 5	0x0000	0x0000	0x0000	Retired
6	0x003F	0x003F	0x003F	Number of logical sectors per logical track
7 - 8	0x0000	0x0000	0x0000	Reserved
9	0x0000	0x0000	0x0000	Retired
10 -19	XXXX	XXXX	XXXX	Serial number(20 ASCII characters)
20 - 21	0x0000	0x0000	0x0000	Retired
22	0x0004	0x0004	0x0004	Obsolete
23 - 26	XXXX	XXXX	XXXX	Firmware revision(8 ASCII characters)
27- 46	XXXX	XXXX	XXXX	Model number
47	0x8010	0x8010	0x8010	Number of sectors on multiple commands
48	0x4000	0x4000	0x4000	Reserved
49	0x2F00	0x2F00	0x2F00	Capabilities
50	0x4000	0x4000	0x4000	Capabilities
51 - 52	0x0200	0x0200	0x0200	Obsolete
53	0x0007	0x0007	0x0007	Reserved
54	0x3FFF	0x3FFF	0x3FFF	Number of current logical cylinders
55	0x0010	0x0010	0x0010	Number of current logical heads
56	0x003F	0x003F	0x003F	Number of current logical sectors per track
57	0xFC10	0xFC10	0xFC10	Current capacity in sectors
58	0x00FB	0x00FB	0x00FB	
59	0x0110	0x0110	0x0110	Multiple sector setting
60	0x0AB0	0xC2B0	0xFFFF	Total number of user addressable sectors (LBA mode only, Compliant with IDEMA Standard)
61	0x0774	0x0EE7	0x0FFF	
62	0x0000	0x0000	0x0000	Obsolete
63	0x0007	0x0007	0x0007	Multi-word DMA transfer
64	0x0003	0x0003	0x0003	Flow control PIO transfer modes supported
65	0x0078	0x0078	0x0078	Minimum Multiword DMA transfer cycle time per word
66	0x0078	0x0078	0x0078	Manufacturer's recommended Multiword DMA transfer cycle time per word
67	0x0078	0x0078	0x0078	Minimum PIO transfer cycle time without flow control
68	0x0078	0x0078	0x0078	Minimum PIO transfer cycle time with IORDY flow control
69 - 74	0x0000	0x0000	0x0000	Reserved
75	0x001F	0x001F	0x001F	No DMA QUEUED command Supports
76	0x0706	0x0706	0x0706	Serial ATA capabilites
77	0x0000	0x0000	0x0000	Reserved for future Serial ATA definition
78	0x004C	0x004C	0x004C	Serial ATA features supported
79	0x0040	0x0040	0x0040	Seral ATA features enabled
80	0x00FC	0x00FC	0x00FC	Major version number
81	0x001A	0x001A	0x001A	Minor version number
82	0x746B	0x746B	0x746B	Command set supported
83	0x7F01	0x7F01	0x7F01	Command set supported
84	0x4163	0x4163	0x4163	Command set/feature supported extension
85	0x7469	0x7469	0x7469	Command set/feature enabled
86	0xBC01	0xBC01	0xBC01	Command set/feature enabled
87	0x4163	0x4163	0x4163	Command set/feature default
88	0x203F	0x203F	0x203F	Ultra DMA transfer
89	0x0003	0x0003	0x0003	Time required for security erase unit completion

Word	64GB	128GB	256GB	Description
90	0x0003	0x0003	0x0003	Time required for Enhanced security erase complete
91	0x0000	0x0000	0x0000	Current advanced power management value
92	0xFFFE	0xFFFE	0xFFFE	Master Password Revision Code
93	0x0000	0x0000	0x0000	Hardware reset result
94	0x8000	0x8000	0x8000	Current automatic acoustic management value
95~97	0x0000	0x0000	0x0000	Reserved
98-99	0x0000	0x0000	0x0000	Reserved
100-103	0x07740AB0	0x0EE7C2B0	0x1DCF32B0	Maximum user LBA for 48bit Address feature set (Compliant with IDEMA Standard)
104	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
105	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
106	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
107	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
108-111	XXXX	XXXX	XXXX	Compliant with IDEMA Standard
112-115	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
116	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
117-118	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
119	0x4014	0x4014	0x4014	Compliant with IDEMA Standard
120	0x4014	0x4014	0x4014	Compliant with IDEMA Standard
121-126	0x0000	0x0000	0x0000	Compliant with IDEMA Standard
127	0x0000	0x0000	0x0000	Removable Media Status Notification feature set supported
128	0x0021	0x0021	0x0021	Security status
129-159	0x0000	0x0000	0x0000	Reserved
160	0x0000	0x0000	0x0000	CFA power mode1
161-175	0x0000	0x0000	0x0000	Reserved
176-205	0x0000	0x0000	0x0000	Current media serial number
206	0x0000	0x0000	0x0000	Reserved
207-208	0x0000	0x0000	0x0000	Reserved
209	0x0000	0x0000	0x0000	Reserved
210-211	0x0000	0x0000	0x0000	Reserved
212-213	0x0000	0x0000	0x0000	Reserved
214	0x0000	0x0000	0x0000	Reserved
216	0x0000	0x0000	0x0000	Reserved
217	0x0001	0x0001	0x0001	Reserved
218	0x0000	0x0000	0x0000	Reserved
219	0x0000	0x0000	0x0000	Reserved
220	0x0000	0x0000	0x0000	Reserved
221	0x0000	0x0000	0x0000	Reserved
222	0x0000	0x0000	0x0000	Reserved
223	0x0000	0x0000	0x0000	Reserved
224-233	0x0000	0x0000	0x0000	Reserved
234	0x0000	0x0000	0x0000	Reserved
235	0x0180	0x0180	0x0180	Reserved
236-254	0x0000	0x0000	0x0000	Reserved
255	0x77A5	0x13A5	0x15A5	Integrity word

11.0 Ordering Information

MMXXXXXXXXXX - XXXXX
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Module: M

2. Card: M

3~4. Flash Density

5. Feature
E : NSSD

6~8. NSSD Density

9. NSSD Type
8 : 1.8" Formfator

10. Component Generation

11. Flash Package

12. PCB Revision AND Production Site

13. " - "

14. Packing Type

15. Controller

16. Controller Firmware Revision

17 ~ 18. Customer Grade

12.0 Product Line up

Part Number	Density	Type	Remark
MMDPE56G8DXP-0VB	256GB	1.8"	
MMCRE28G8MXP-0VB	128GB	1.8"	
MMCRE64G8MXP-0VB	64GB	1.8"	