ESP32-S2-WROVER
ESP32-S2-WROVER-I

Datasheet Version 1.4

END OF LIFE (EOL)

2.4 GHz Wi-Fi (802.11 b/g/n) module
Built around ESP32-S2 series of SoC (chip revision 0), Xtensa® single-core 32-bit LX7 microprocessor
Flash up to 16 MB, 2 MB PSRAM
37 GPIOs, rich set of peripherals
On-board PCB antenna or external antenna connector



ESP32-S2-WROVER



ESP32-S2-WROVER-I

ESPRESSIF

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document: https://www.espressif.com/documentation/esp32-s2-wrover_esp32-s2-wrover-i_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32-S2 embedded, Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Operating frequency: 2412 ~ 2484 MHz

Peripherals

- GPIO, SPI, LCD, UART, I2C, I2S, Camera interface, IR, pulse counter, LED PWM, TWAI® (compatible with ISO 11898-1, i.e. CAN Specification 2.0), full-speed USB OTG, ADC, DAC, touch sensor, temperature sensor

Note:

* Please refer to *ESP32-S2 Series Datasheet* for detailed information about the module peripherals.

Integrated Components on Module

- 40 MHz crystal oscillator
- 4 MB SPI flash
- 2 MB PSRAM

Antenna Options

- On-board PCB antenna (ESP32-S2-WROVER)
- External antenna via a connector (ESP32-S2-WROVER-I)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: –40 ~ 85 °C

Certification

- RF certification: See certificates for ESP32-S2-WROVER and ESP32-S2-WROVER-I
- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Description

ESP32-S2-WROVER and ESP32-S2-WROVER-I are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios related to Internet of Things (IoT), such as embedded systems, smart home, wearable electronics, etc.

ESP32-S2-WROVER comes with a PCB antenna (ANT). ESP32-S2-WROVER-I comes with a connector for an external antenna (CONN).

They both feature a 4 MB external SPI flash and an additional 2 MB SPI Pseudo static RAM (PSRAM). The information in this datasheet is applicable to both modules.

The ordering information for the two modules is as follows:

Table 1: Ordering Information

Module	Chip Embedded	Flash	PSRAM	Chip Revision	Module Dimensions (mm)
ESP32-S2-WROVER (ANT) (EOL)	ESP32-S2	4 MB	2 MB	v1.0	18.0 × 31.0 × 3.3
ESP32-S2-WROVER-I (CONN) (EOL)					

At the core of the modules is ESP32-S2 *, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. You can power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds.

ESP32-S2 integrates a rich set of peripherals including SPI, I2S, UART, I2C, LED PWM, TWAI® controller, ADC, DAC, touch sensor, temperature sensor, as well as up to 43 GPIOs. It also includes a full-speed USB OTG (OTG) interface to enable USB communication.

Note:
* For more information on ESP32-S2, please refer to *ESP32-S2 Series Datasheet*.

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Home Control Panel
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications
- Smart POS Machines

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2 Block Diagram

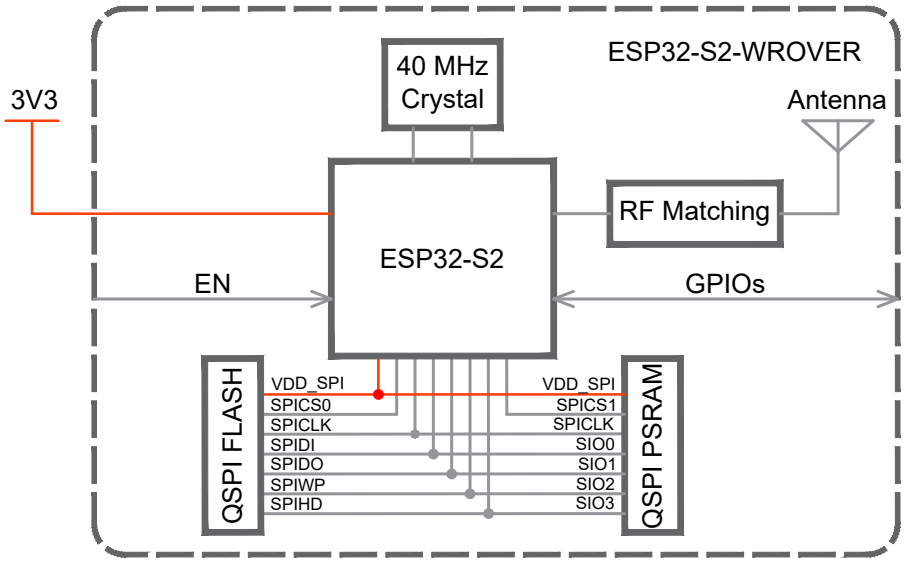


Figure 1: ESP32-S2-WROVER Block Diagram

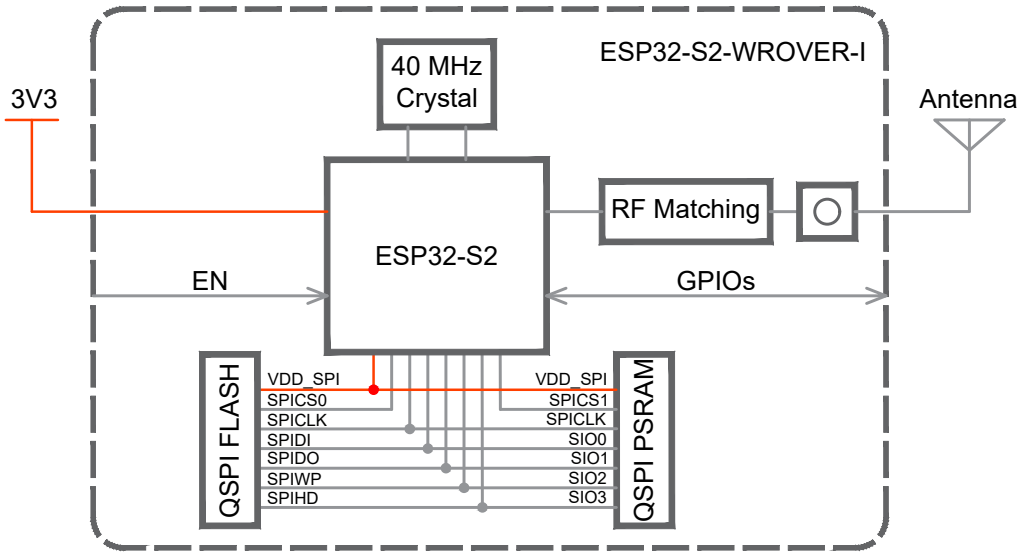


Figure 2: ESP32-S2-WROVER-I Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 7.1 *Physical Dimensions*.

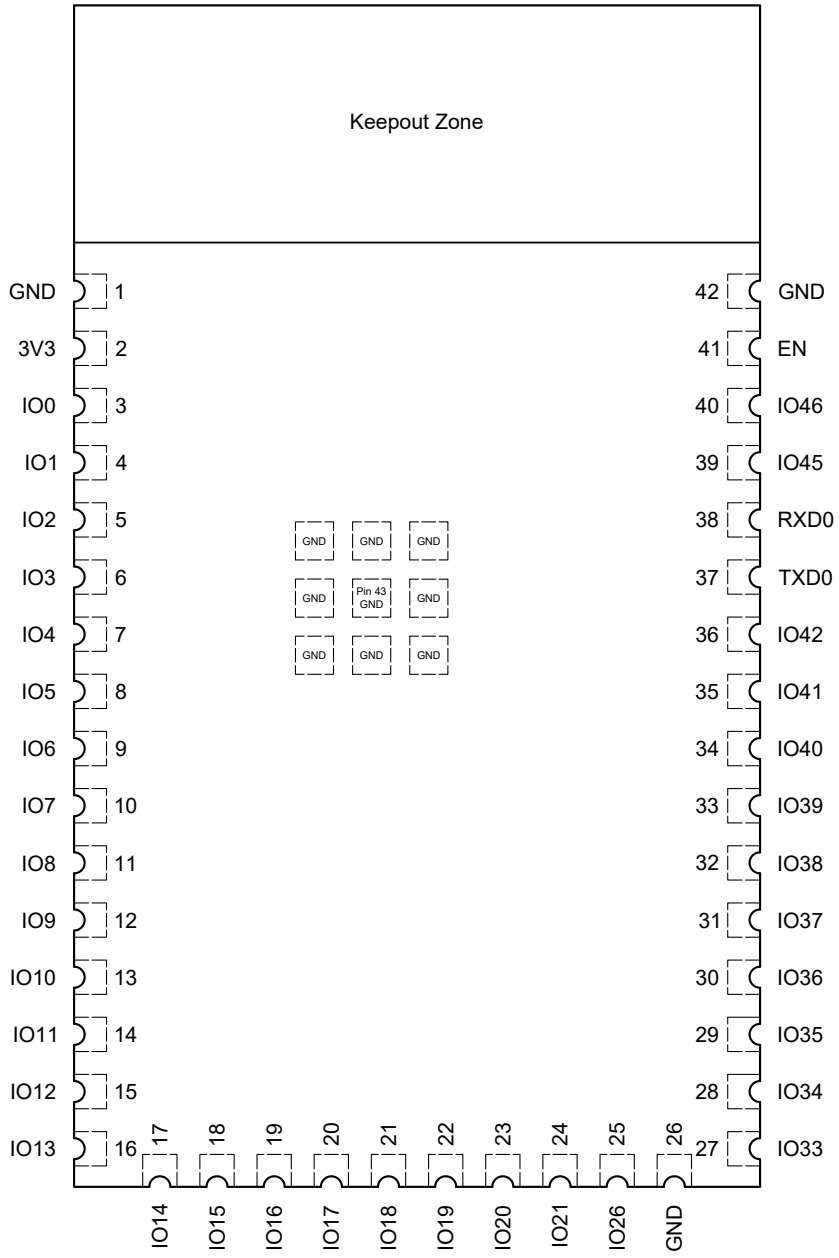


Figure 3: Pin Layout (Top View)

3.2 Pin Description

The module has 42 pins. See pin definitions in Table 2 *Pin Definitions*.

For peripheral pin configurations, please refer to *ESP32-S2 Series Datasheet* > Section *Peripheral Pin Configurations*.

Table 2: Pin Definitions

Name	No.	Type[1]	Function
GND	1	P	Ground
3V3	2	P	Power supply
IO0	3	I/O/T	RTC_GPIO0, GPIO0
IO1	4	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
IO2	5	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO3	6	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO4	7	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	8	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	9	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	10	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO8	11	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
IO9	12	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
IO10	13	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPII04
IO11	14	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPII05
IO12	15	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPII06
IO13	16	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPII07
IO14	17	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
IO15	18	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	19	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	20	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
IO18	21	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
IO19	22	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	23	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO21	24	I/O/T	RTC_GPIO21, GPIO21
IO26	25	I/O/T	SPICS1, GPIO26 [2]
GND	26	P	Ground
IO33	27	I/O/T	SPII04, GPIO33, FSPIHD
IO34	28	I/O/T	SPII05, GPIO34, FSPICS0
IO35	29	I/O/T	SPII06, GPIO35, FSPID
IO36	30	I/O/T	SPII07, GPIO36, FSPICLK
IO37	31	I/O/T	SPIDQS, GPIO37, FSPIQ
IO38	32	I/O/T	GPIO38, FSPIWP
IO39	33	I/O/T	MTCK, GPIO39, CLK_OUT3
IO40	34	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	35	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	36	I/O/T	MTMS, GPIO42
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
RXD0	38	I/O/T	U0RXD, GPIO44, CLK_OUT2
IO45	39	I/O/T	GPIO45
IO46	40	I	GPIO46

Cont'd on next page

Table 2 – cont'd from previous page

Name	No.	Type[1]	Function
EN	41	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
GND	42	P	Ground

[1] P: power supply; I: input; O: output; T: high impedance.

[2] By default, IO26 is connected to the CS pin of the PSRAM and cannot be used for other functions.

3.3 Strapping Pins

Note:

The content below is excerpted from *ESP32-S2 Series Datasheet* > Section *Strapping Pins*. For the strapping pin mapping between the chip and modules, please refer to Chapter 5 *Module Schematics*.

At each startup or reset, a module requires some initial configuration parameters, such as in which boot mode to load the module, voltage of flash memory, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

The parameters controlled by the given strapping pins at module reset are as follows:

- **Chip boot mode** – GPIO0 and GPIO46
- **VDD_SPI voltage** – GPIO45
- **ROM messages printing** – GPIO46

GPIO0, GPIO45, and GPIO46 are connected to the chip's internal weak pull-up/pull-down resistors at chip reset. These resistors determine the default bit values of the strapping pins. Also, these resistors determine the bit values if the strapping pins are connected to an external high-impedance circuit.

Table 3: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO45	Pull-down	0
GPIO46	Pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S2 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 4 and Figure 4.

Table 4: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

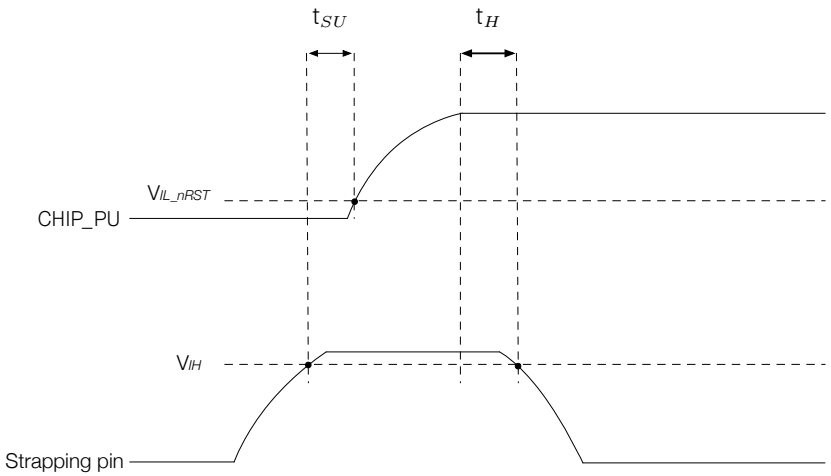


Figure 4: Visualization of Timing Parameters for the Strapping Pins

3.3.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 5 Chip Boot Mode Control.

Table 5: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default configuration	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Download Boot	0	0
Invalid combination [1]	0	1

[1] This combination triggers unexpected behavior and should be avoided.

3.3.2 VDD_SPI Voltage Control

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 6: VDD_SPI Voltage Control

EFUSE_VDD_SPI_FORCE	GPIO45	eFuse [1]	Voltage	VDD_SPI power source [2]
0	0	Ignored	3.3 V	VDD3P3_RTC_IO via R_{SPI}
	1		1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
		1	3.3 V	VDD3P3_RTC_IO via R_{SPI}

[1] eFuse: EFUSE_VDD_SPI_TIEH

[2] See *ESP32-S2 Series Datasheet* > Section *Power Scheme*

3.3.3 ROM Messages Printing Control

During boot process the messages by the ROM code can be printed to:

- **(Default) U0TXD pin.** For this, EFUSE_UART_PRINT_CONTROL should be 0.
- **DAC_1 pin.** For this, EFUSE_UART_PRINT_CONTROL should be 1.

EFUSE_UART_PRINT_CONTROL and GPIO46 control ROM messages printing as shown in Table 7 ROM Messages Printing Control.

Table 7: ROM Messages Printing Control

eFuse[1]	GPIO46	ROM Messages Printing
0	Ignored	Always enabled
1	0	Enabled
	1	Disabled
2	0	Disabled
	1	Enabled
3	Ignored	Always disabled

[1] eFuse: EFUSE_UART_PRINT_CONTROL

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in Table 8 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 9 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	85	°C

4.2 Recommended Operating Conditions

Table 9: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	−40	—	85	°C

4.3 DC Characteristics (3.3 V, 25 °C)

Table 10: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage	−0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.
[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.4 Current Consumption Characteristics

Owing to the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *RTC and Low-Power Management* in *ESP32-S2 Series Datasheet*.

Table 11: Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	340
		802.11g, 20 MHz, 54 Mbps, @15 dBm	315
		802.11n, 20 MHz, MCS7, @13.5 dBm	298
		802.11n, 40 MHz, MCS7, @13.5 dBm	300
	RX	802.11b/g/n, 20 MHz	81
		802.11n, 40 MHz	88

[1] The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on 100% duty cycle.
[2] The current consumption figures in RX mode are for cases where the peripherals are disabled and the CPU idle.

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S2 Series Datasheet*.

4.4.1 Current Consumption in Other Modes

The measurements below are applicable to ESP32-S2, ESP32-S2FH2, and ESP32-S2FH4. Since ESP32-S2FN4R2 and ESP32-S2R2 come with in-package PSRAM, their current consumption might be higher.

Table 12: Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ	
			All Peripherals Clocks Disabled (mA)	All Peripherals Clocks Enabled (mA)[1]
Modem-sleep[2,3]	240	CPU is idle	20.0	28.0
		CPU is running	23.0	32.0
	160	CPU is idle	14.0	21.0
		CPU is running	16.0	24.0
	80	CPU is idle	10.5	18.4
		CPU is running	12.0	20.0

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Table 12 – cont'd from previous page

Mode	CPU Frequency (MHz)	Description	Typ	
			All Peripherals Clocks Disabled (mA)	All Peripherals Clocks Enabled (mA)[1]

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 13: Current Consumption in Low-Power Modes

Work mode	Description		Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance		750
Deep-sleep	The ULP co-processor is powered on[2]	ULP-FSM	170
		ULP-RISC-V	190
	ULP sensor-monitored pattern[3]		22
	RTC timer + RTC memory		25
	RTC timer only		20
Power off	CHIP_PU is set to low level, the chip is powered off		1

[1] In Light-sleep mode, with all related SPI pins pulled up, the current consumption of the embedded PSRAM is 140 μA. Chip variants with in-package PSRAM include ESP32-S2FN4R2 and ESP32-S2R2.

[2] During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I2C are able to operate.

[3] The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 22 μA.

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 14: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel [1]		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	802.11b: 1, 2, 5.5 and 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	802.11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna, external antenna connector

[1] Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.

[2] For the modules that use external antenna connectors, the output impedance is 50 Ω. For other modules without external antenna connectors, the output impedance is irrelevant.

4.5.2 Transmitter Characteristics

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 15.

Table 15: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	–	19.5	–
802.11b, 11 Mbps, CCK	–	19.5	–
802.11g, 6 Mbps, OFDM	–	18.0	–
802.11g, 54 Mbps, OFDM	–	17.5	–
802.11n, HT20, MCS0	–	18.0	–
802.11n, HT20, MCS7	–	17.0	–
802.11n, HT40, MCS0	–	18.0	–
802.11n, HT40, MCS7	–	16.5	–

Table 16: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	–	-24.0	-10.0
802.11b, 11 Mbps, CCK	–	-24.0	-10.0
802.11g, 6 Mbps, OFDM	–	-25.0	-5.0
802.11g, 54 Mbps, OFDM	–	-28.0	-25.0
802.11n, HT20, MCS0	–	-25.0	-5.0
802.11n, HT20, MCS7	–	-30.0	-27.0
802.11n, HT40, MCS0	–	-25.0	-5.0
802.11n, HT40, MCS7	–	-30.0	-27.0

[1] EVM is measured at the corresponding typical TX power provided in Table 15 *TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

4.5.3 Receiver Characteristics

Table 17: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	–	-96.0	–
802.11b, 2 Mbps, DSSS	–	-93.5	–
802.11b, 5.5 Mbps, CCK	–	-91.5	–
802.11b, 11 Mbps, CCK	–	-87.0	–
802.11g, 6 Mbps, OFDM	–	-91.5	–

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Table 17 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11g, 9 Mbps, OFDM	—	–90.0	—
802.11g, 12 Mbps, OFDM	—	–88.0	—
802.11g, 18 Mbps, OFDM	—	–86.0	—
802.11g, 24 Mbps, OFDM	—	–83.0	—
802.11g, 36 Mbps, OFDM	—	–79.0	—
802.11g, 48 Mbps, OFDM	—	–75.0	—
802.11g, 54 Mbps, OFDM	—	–73.5	—
802.11n, HT20, MCS0	—	–91.0	—
802.11n, HT20, MCS1	—	–87.5	—
802.11n, HT20, MCS2	—	–85.0	—
802.11n, HT20, MCS3	—	–82.0	—
802.11n, HT20, MCS4	—	–78.5	—
802.11n, HT20, MCS5	—	–74.5	—
802.11n, HT20, MCS6	—	–72.5	—
802.11n, HT20, MCS7	—	–71.5	—
802.11n, HT40, MCS0	—	–87.5	—
802.11n, HT40, MCS1	—	–85.0	—
802.11n, HT40, MCS2	—	–82.5	—
802.11n, HT40, MCS3	—	–78.5	—
802.11n, HT40, MCS4	—	–75.0	—
802.11n, HT40, MCS5	—	–71.0	—
802.11n, HT40, MCS6	—	–69.5	—
802.11n, HT40, MCS7	—	–68.5	—

Table 18: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 19: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	35	—
802.11b, 11 Mbps, CCK	—	35	—
802.11g, 6 Mbps, OFDM	—	31	—
802.11g, 54 Mbps, OFDM	—	14	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	13	—
802.11n, HT40, MCS0	—	19	—
802.11n, HT40, MCS7	—	8	—

5 Module Schematics

This is the reference design of the module.

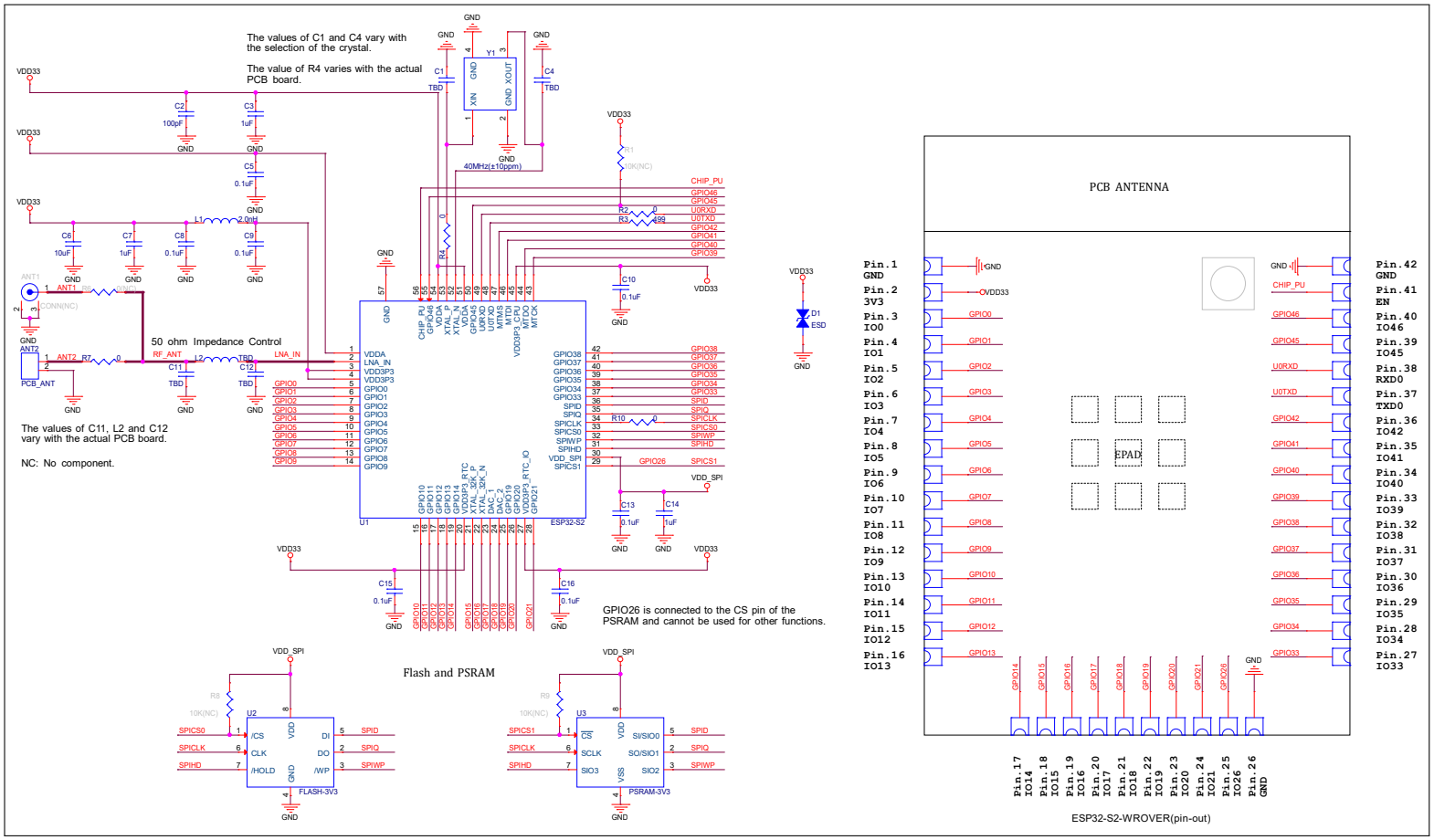


Figure 5: ESP32-S2-WROVER Schematics

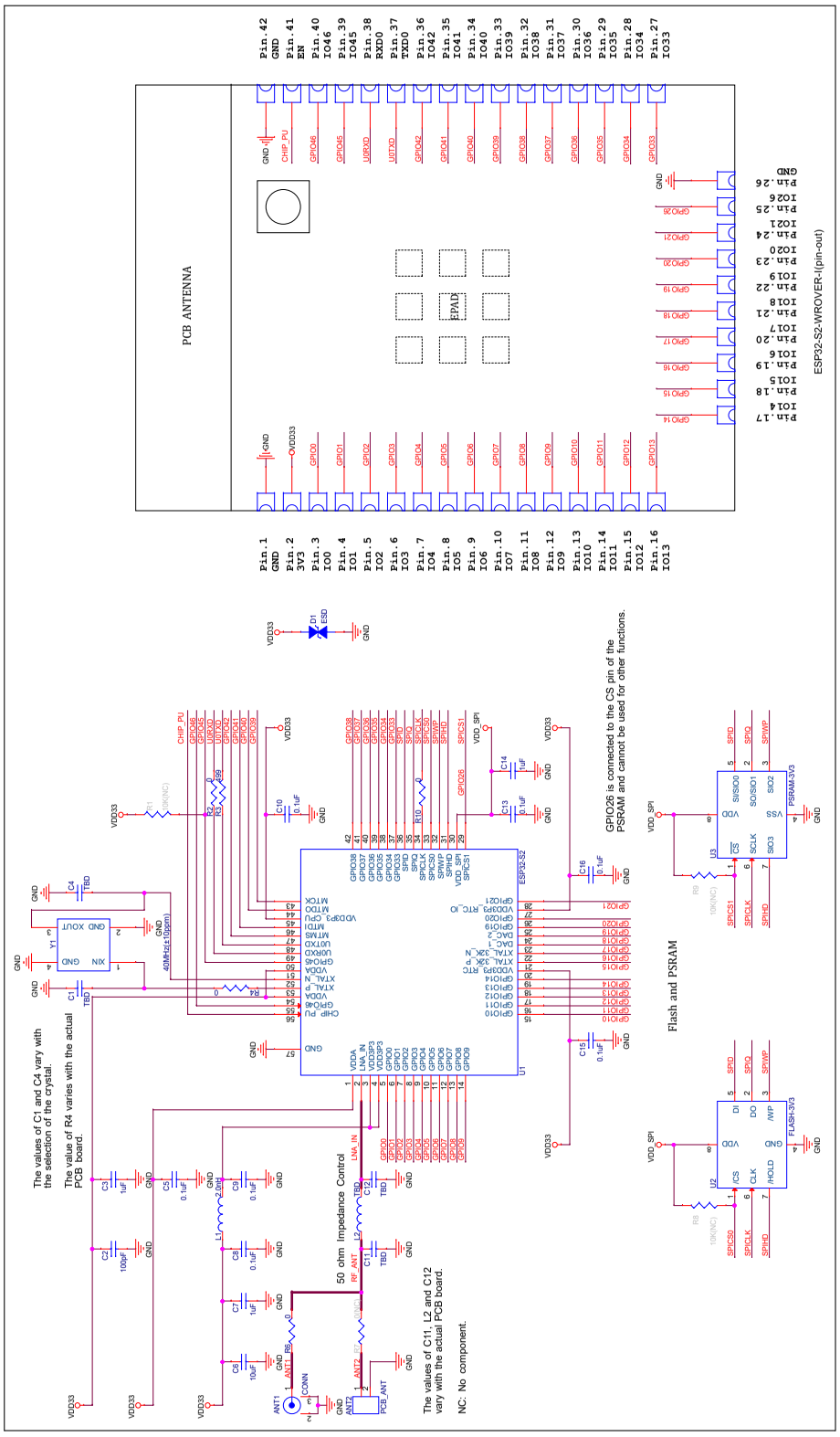


Figure 6: ESP32-S2-WROVER-I Schematics

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

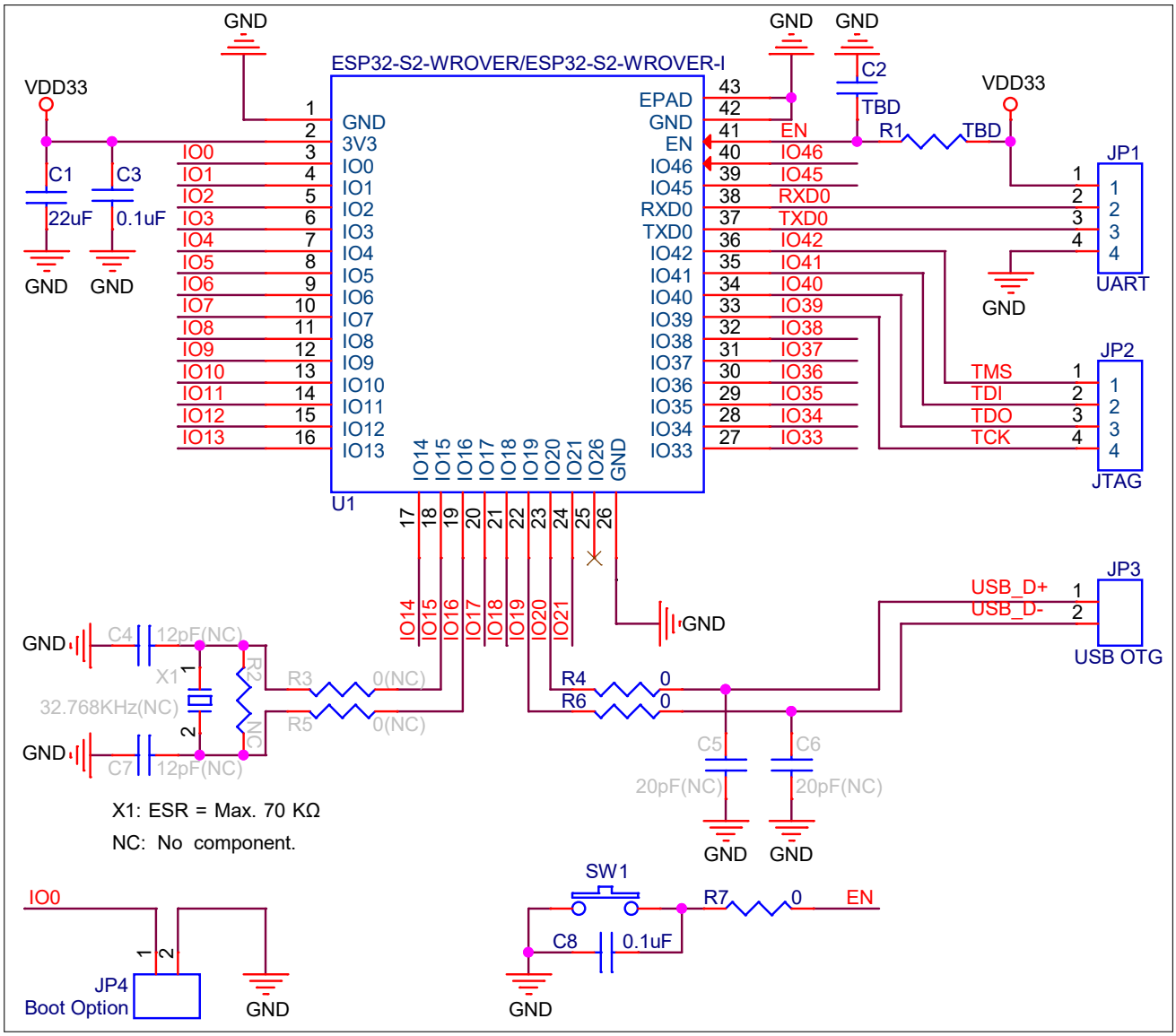


Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S2 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to *ESP32-S2 Series Datasheet* > Section *Power Scheme*.

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

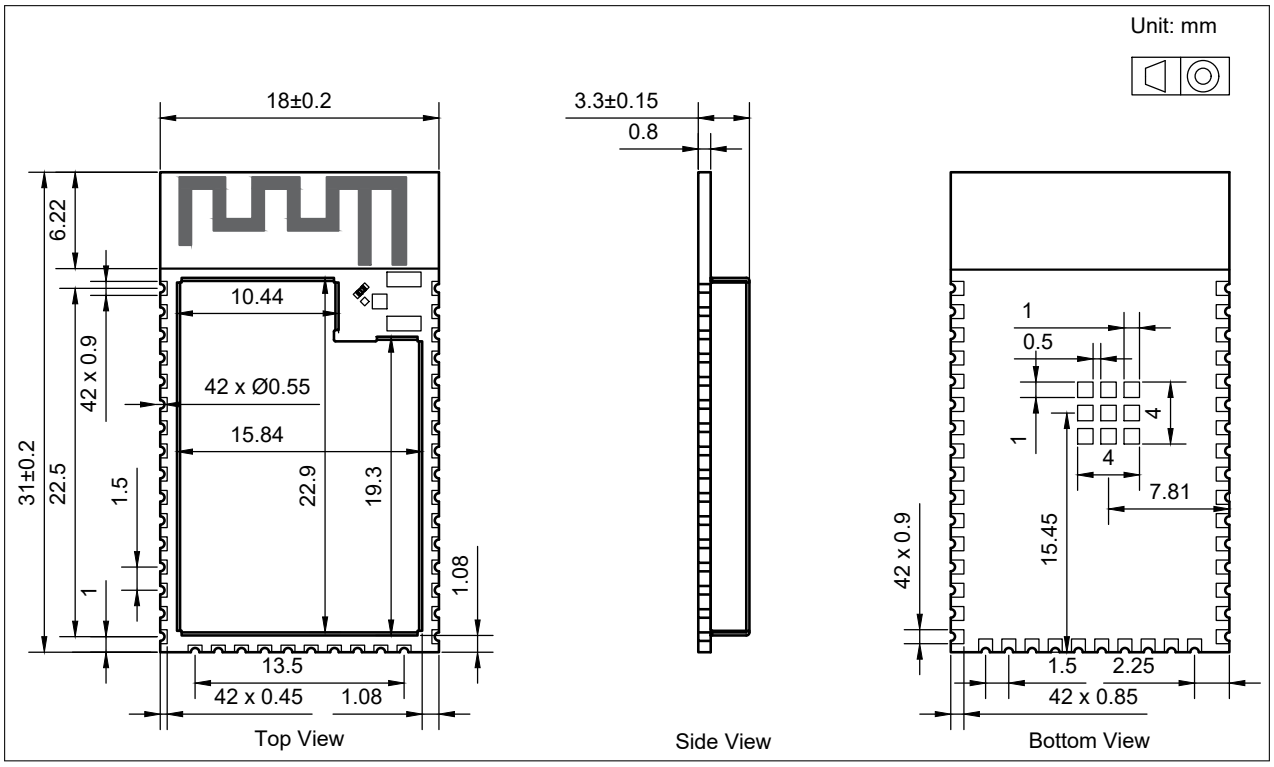


Figure 8: ESP32-S2-WROVER Physical Dimensions

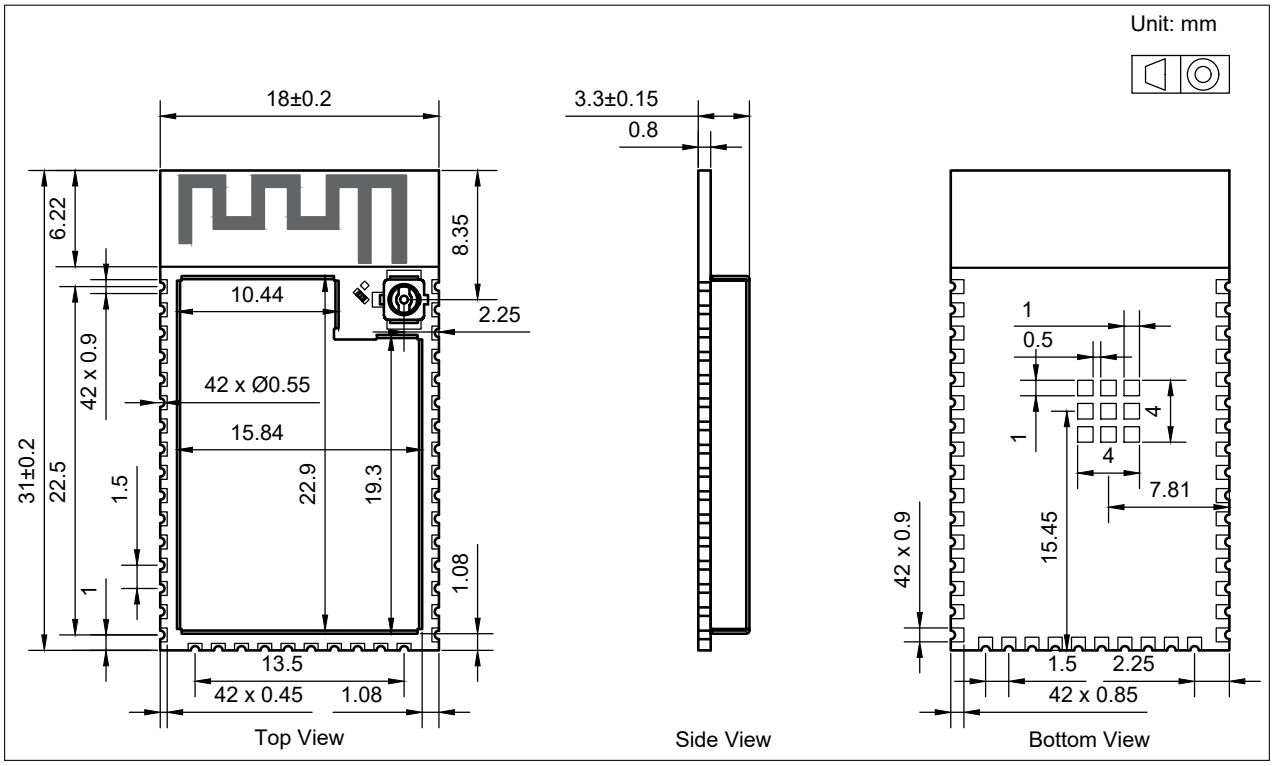


Figure 9: ESP32-S2-WROVER-I Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to *Espressif Module Packaging Information*.

7.2 Recommended PCB Land Pattern

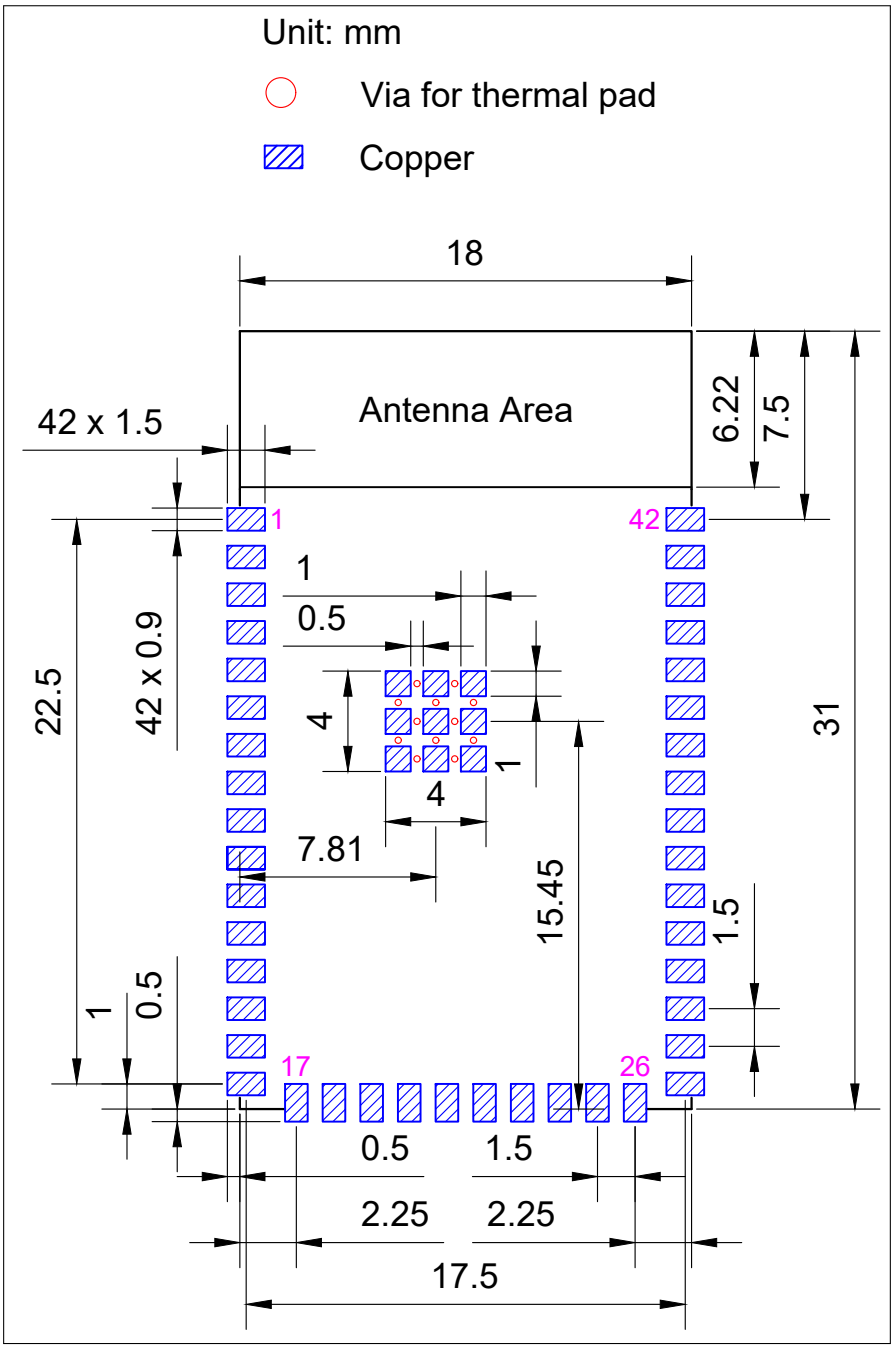


Figure 10: Recommended PCB Land Pattern

7.3 Dimensions of External Antenna Connector

ESP32-S2-WROVER-I uses the first generation external antenna connector as shown in Figure 11 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

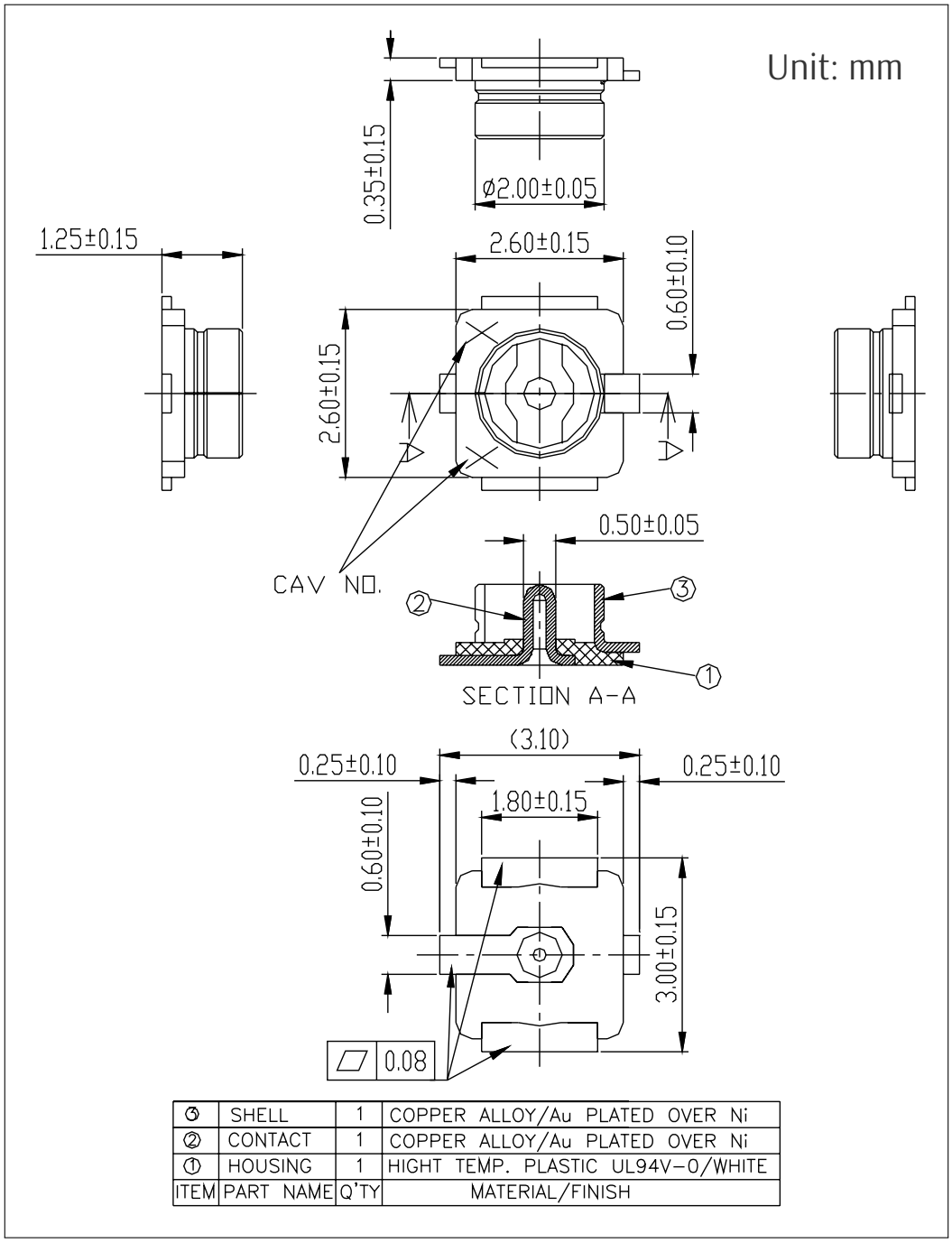


Figure 11: Dimensions of External Antenna Connector

8 Product Handling

8.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

8.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

8.3 Soldering Profile

8.3.1 Reflow Profile

Solder the module in a single reflow.

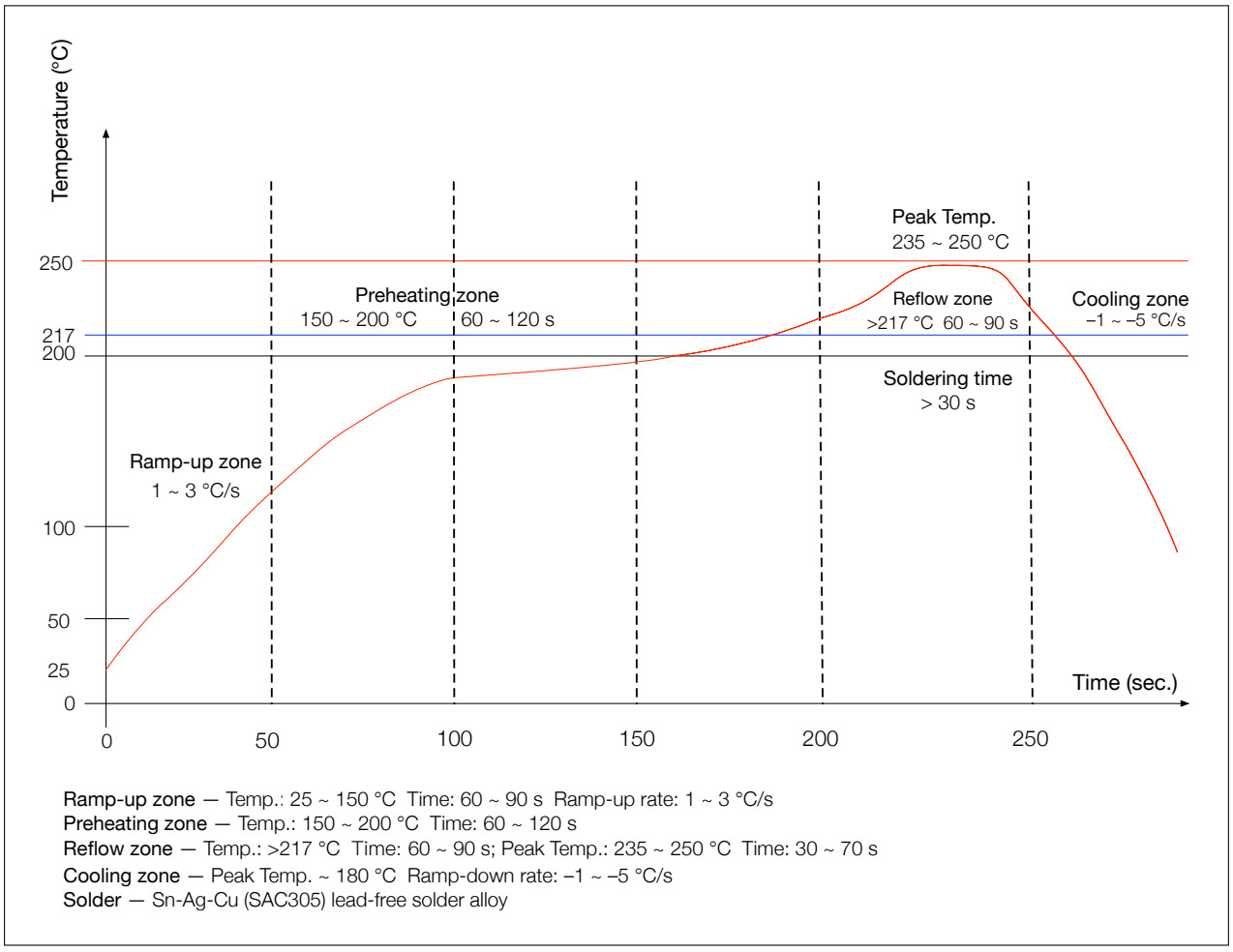


Figure 12: Reflow Profile

8.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

9 MAC Addresses and eFuse

The eFuse in ESP32-S2 series of chips has been burnt into 48-bit mac_address. The actual addresses the chip uses in station or AP modes correspond to mac_address in the following way:

- Station mode: mac_address
- AP mode: mac_address + 1

There are seven blocks in eFuse for users to use. Each block is 256 bits in size and has independent write/read disable controller. Six of them can be used to store encrypted key or user data, and the remaining one is only used to store user data.

Related Documentation and Resources

Related Documentation

- ESP32-S2 Series Datasheet – Specifications of the ESP32-S2 hardware.
- ESP32-S2 Technical Reference Manual – Detailed information on how to use the ESP32-S2 memory and peripherals.
- ESP32-S2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S2 into your hardware product.
- ESP32-S2 Series SoC Errata – Descriptions of known errors in ESP32-S2 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S2
- *ESP32-S2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S2 Series SoCs* – Browse through all ESP32-S2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S2
- *ESP32-S2 Series Modules* – Browse through all ESP32-S2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S2
- *ESP32-S2 Series DevKits* – Browse through all ESP32-S2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2025-02-24	v1.4	• Marked ESP32-S2-WROVER as end of life. Note this datasheet is no longer maintained.
2024-09-05	v1.3	• According to PCN20230702, upgraded the chip ESP32-S2 from chip revision v0.0 to chip revision v1.0 • Marked ESP32-S2-WROVER-I as end of life • Updated performance data tables in Section 4 *Electrical Characteristics* • Updated peripheral schematic in Chapter 6 *Peripheral Schematics*
2022-03-01	v1.2	• Added module introduction and pictures on the title page • Added NRND watermark • Added a note with a link and QR code to the latest version of the document • Updated Section "Learning Resources" and renamed to "Related Documentation and Resources" • Updated Table 12 *Current Consumption in Modem-sleep Mode* and Table 13 *Current Consumption in Low-Power Modes*
2020-12-17	v1.1	• Added TWAI to Chapter 1 *Module Overview* • Updated Table 11 *Current Consumption Depending on RF Modes* • Updated the capacitance value of RC delay circuit to 1 μF in Chapter 6 *Peripheral Schematics* • Updated note in Section 8.3.1 *Reflow Profile*
2020-06-01	v1.0	Official release
2020-03-10	v0.5	Preliminary release



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End of Life (EOL)