19-4699; 7/09

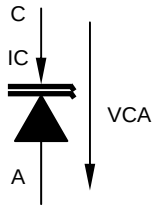
DS9503
ESD Protection Diode with Resistors

www.maxim-ic.com

SPECIAL FEATURES

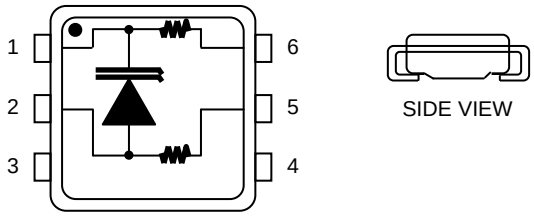
- Zener characteristic with voltage snap–back to protect against ESD hits
- High avalanche voltage, low leakage and low capacitance avoid signal attenuation
- Compatible to all 5V logic families
- Space saving, low inductance TSOC surface mount package
- On–chip 5Ω resistors for isolation at both anode and cathode terminals
- Industrial temperature range

SYMBOL AND CONVENTIONS



PACKAGE OUTLINE

TSOC SURFACE MOUNT PACKAGE



TOP VIEW

ORDERING INFORMATION

DS9503P+	6-lead TSOC package
DS9503P+T&R	6-lead TSOC package

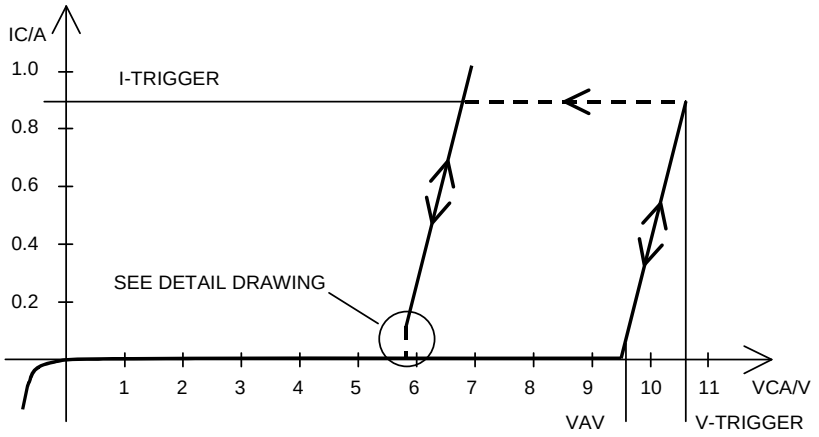
+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

DESCRIPTION

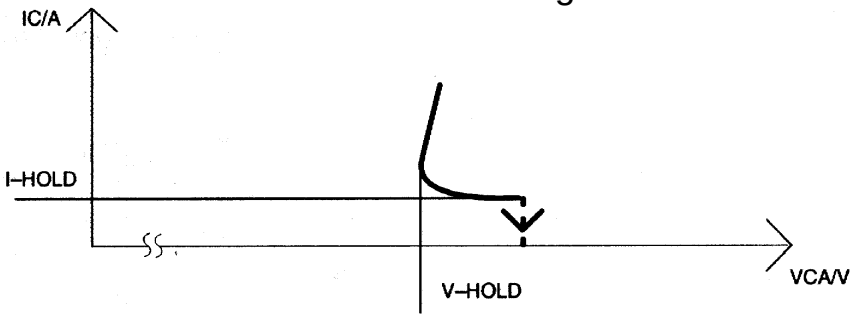
This DS9503 is designed as an ESD protection device for 1–Wire MicroLAN interfaces. In contrast to the DS9502, the DS9503 includes two 5Ω isolation resistors on chip. Although 5Ω are negligible during communication, they represent a high impedance relative to the conducting diode during an ESD event. Thus, the diode absorbs the energy while the resistors further isolate and protect the circuit at the other side of the package. If used with circuits that already have a strong ESD–protection at their I/O port, the ESD protection level is raised to more that 27 kV (IEC 801–2 Reference model). In case of abnormal ESD hits beyond its maximum ratings the DS9503 will eventually fail “short” thus preventing further damage.

During normal operation the DS9503 behaves like a regular Zener Diode. When the voltage exceeds the trigger voltage, the I/V characteristic of the device will “snapback” allowing the same or higher amount of current to flow, but at a significantly lower voltage. As long as a minimum current or voltage is maintained, the device will stay in the “snapback mode”. If the voltage or the current falls below the holding voltage or holding current, the device will abruptly change to its normal mode and conduct only a small leakage current.

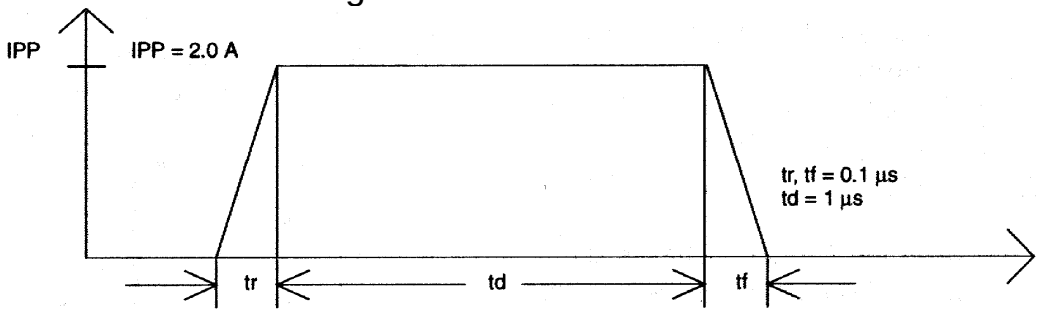
DC CHARACTERISTICS Figure 1



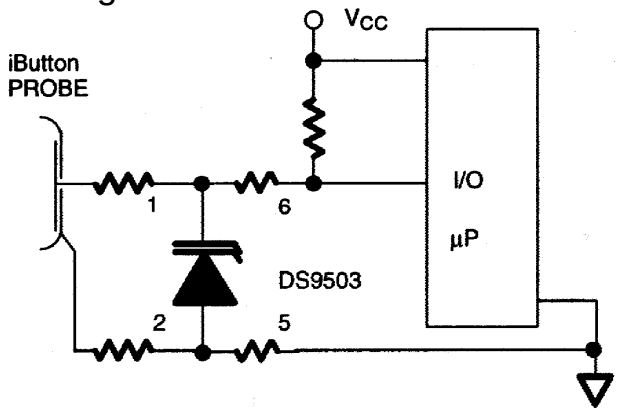
DC CHARACTERISTICS DETAIL DRAWING Figure 2



TEST PULSE WAVEFORM Figure 3



TYPICAL APPLICATION Figure 4



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Continuous DC Current Through Package	80 mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability

ELECTRICAL CHARACTERISTICS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Leakage Current	I_L		30	100	nA	1
Avalanche Voltage	V_{AV}	7.4		11.05	V	2,3
Trigger Voltage	$V_{TRIGGER}$		10	11	V	2, 4
Trigger Current	$I_{TRIGGER}$			1000	mA	4
Holding Voltage	V_{HOLD}	5.5			V	2,4
Holding Current	I_{HOLD}	11			mA	4
Forward Voltage (-10 mA)	V_F		-0.7	-0.8	V	5
Forward Current (-0.7V)	I_F		-10	-100	mA	5
Maximum Peak Current	I_{PP}		2.0		A	6
Continuous Current Through Diode	I_{CC}			±80	mA	
Isolation Resistance	R_I		5		Ω	

CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Junction Capacitance (5V)	C_{J5}		40		pF	2
Junction Capacitance (0V)	C_{J0}		70		pF	2

THERMAL RESISTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Junction To Package	$R_{\Theta JC}$			75	K/W	
Junction To Ambient	$R_{\Theta JA}$			200	K/W	

NOTES:

1. At 7.0V.
2. All voltages are referenced from Cathode to Anode.
3. At 0.3 μA.
4. Not production tested, guaranteed by design.
5. Typical values at room temperature.
6. See pulse specification.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
072209	Added “lead-free” note to the *Ordering Information* table.	1
	Fixed the X/Y scale in Figure 1.	2
	In the *Electrical Characteristics* table, changed the V_{AV} specification maximum value to 11V; the $V_{TRIGGER}$ specification typical value to 10V and maximum value to 11V; the $I_{TRIGGER}$ specification typical value to a blank; and the IH_{OLD} specification minimum value to an 11mA.	3
	Added note 4 (“Not production tested, guaranteed by design”) to the $V_{TRIGGER}$, $I_{TRIGGER}$, V_{HOLD}, and I_{HOLD} specifications in the *Electrical Characteristics* table.	3