CS5460A

Single Phase, Bi-directional Power/Energy IC

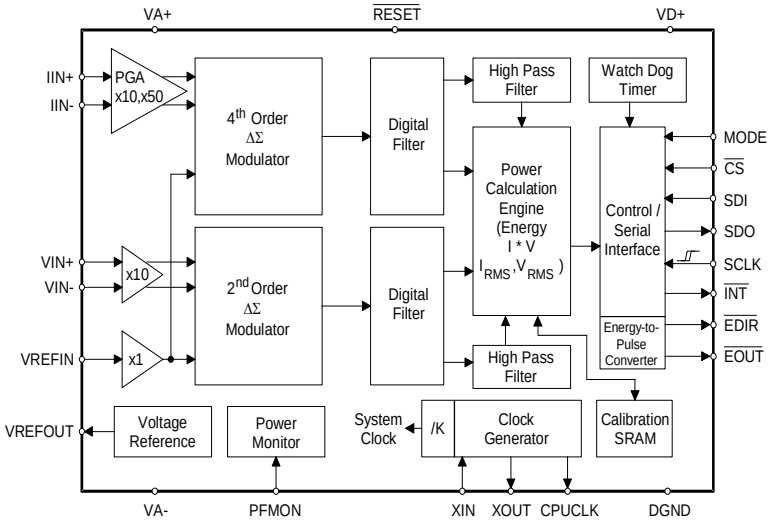
Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range.
- On-Chip Functions: (Real) Energy, I ∗ V, I_{RMS} and V_{RMS}, Energy-to-Pulse Conversion
- Smart "Auto-boot" Mode from Serial EEPROM Enables Use without MCU.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Typical Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- *V* vs. *I* Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/°C drift)
- Simple Three-wire Digital Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3.3 V to +5 V

Description

The CS5460A is a highly integrated power measurement solution which combines two ΔΣ Analog-to-digital Converters (ADCs), high-speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Real (True) Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low-cost shunt resistor or transformer to measure current, and to a resistive divider or potential transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a microcontroller and a pulse output engine for which the average pulse frequency is proportional to the real power. The CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-boot" feature allows the CS5460A to function 'stand-alone' and to initialize itself on system power-up. In Auto-boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can operate without a microcontroller, in order to lower the total bill-of-materials cost.



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1. CHARACTERISTICS & SPECIFICATIONS

ANALOG CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = +5 V ±10%; VREFIN = +2.5 V; VA- = AGND = 0 V; MCLK = 4.096 MHz, K = 1; N = 4000 ==> OWR = 4000 Sps.)(See Notes 1, 2, 3, 4, and 5.)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Analog Inputs (Current Channel)						
Maximum Differential Input Voltage Range {(V_{IIN+}) - (V_{IIN-})}	(Gain = 10) (Gain = 50)	I_{IN}	- -	- -	500 100	mV_{P-P} mV_{P-P}
Total Harmonic Distortion		THD_I	80	-	-	dB
Common Mode + Signal on IIN+ or IIN-	(Gain = 10 or 50)		-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	C_{in}	- -	25 25	- -	pF pF
Effective Input Impedance	(Note 6) (Gain = 10) (Gain = 50)	 Z_{inI} Z_{inI}	 - -	 30 30	 - -	 kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)		- -	- -	20 4	μV_{rms} μV_{rms}
Accuracy (Current Channel)						
Bipolar Offset Error	(Note 1)	VOS_I	-	±0.001	-	%F.S.
Full-Scale Error	(Note 1)	FSE_I	-	±0.001	-	%F.S.
Analog Inputs (Voltage Channel)						
Maximum Differential Input Voltage Range	{(V_{VIN+}) - (V_{VIN-})}	V_{IN}	-	-	500	mV_{P-P}
Total Harmonic Distortion		THD_V	62	-	-	dB
Common Mode + Signal on VIN+ or VIN-			VA-	-	VA+	V
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance		C_{inV}	-	0.2	-	pF
Effective Input Impedance	(Note 6)	Z_{inV}	-	5	-	MΩ
Noise (Referred to Input)			-	-	250	μV_{rms}
Accuracy (Voltage Channel)						
Bipolar Offset Error	(Note 1)	VOS_V	-	±0.01	-	%F.S.
Full-Scale Error	(Note 1)	FSE_V	-	±0.01	-	%F.S.

Notes:
1. Bipolar Offset Errors and Full-Scale Gain Errors for the current and voltage channels refer to the respective Irms Register and Vrms Register output, when the device is operating in 'continuous computation cycles' data acquisition mode, *after* offset/gain system calibration sequences have been executed. These specs do *not* apply to the error of the Instantaneous Current/Voltage Register output.
2. Specifications guaranteed by design, characterization, and/or test.
3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.
4. In requiring VA+ = VD+ =5 V ±10%, note that it is allowable for VA+, VD+ to differ by as much as ±200 mV, as long as VA+ > VD+.
5. Note that "Sps" is an abbreviation for units of "samples per second".
6. Effective Input Impedance (Zin) is determined by clock frequency (DCLK) and Input Capacitance (IC). Zin = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
Phase Compensation Range (Voltage Channel, 60 Hz)			-2.4	-	+2.5	°
High Rate Filter Output Word Rate (Both Channels)		OWR	-	DCLK/1024	-	Sps
Input Sample Rate DCLK = MCLK/K			-	DCLK/8	-	Sps
Full Scale DC Calibration Range (Note 7)		FSCR	25	-	100	%F.S.
Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to “0000000”)				1.0		µs
High Pass Filter Pole Frequency -3 dB			-	0.5	-	Hz
Power Supplies						
Power Supply Currents (Active State)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption (Note 8)	Active State (VD+ = 5 V)	PC	-	21	25	mW
	Active State (VD+ = 3.3 V)		-	11.6	-	mW
	Stand-By State		-	6.75	-	mW
	Sleep State		-	10	-	µW
Power Supply Rejection Ratio for Current Channel (Note 9)	(50, 60 Hz)					
	(Gain = 10)	PSRR	56	-	-	dB
	(Gain = 50)	PSRR	75	-	-	dB
Power Supply Rejection Ratio for Voltage Channel	(50, 60 Hz) (Note 9)	PSRR	-	65	-	dB
PFMON Power-Fail Detect Threshold (Note 10)		PMLO	2.3	2.45	-	V
PFMON “Power-Restored” Detect Threshold (Note 11)		PMHI	-	2.55	2.7	V

Notes:
7. The minimum FSCR is limited by the maximum allowed gain register value.
8. All outputs unloaded. All inputs CMOS level.
9. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV zero-to-peak sinewave (frequency = 60 Hz) is imposed onto the +5 V supply voltage at VA+ and VD+ pins. The “+” and “-” input pins of both input channels are shorted to VA-. Then the CS5460A is commanded to ’continuous computation cycles’ data acquisition mode, and digital output data is collected for the channel under test. The zero-peak value of the digital sinusoidal output signal is determined, and this value is converted into the zero-peak value of the sinusoidal voltage that would need to be applied at the channel’s inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{0.150V}{V_{eq}}\right\}$$

10. When voltage level on PFMON is sagging, and LSD bit is 0, the voltage at which LSD bit is set to 1.
11. Assuming that the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), then if/when the PFMON voltage starts to rise again, PMHI is the voltage level (on PFMON pin) at which the LSD bit can be permanently reset back to 0 (without instantaneously changing back to 1). Attempts to reset the LSD bit before this condition is true will not be successful. This condition indicates that power has been restored. Typically, for a given sample, the PMHI voltage will be ~100 mV above the PMLO voltage.

VREFOUT REFERENCE OUTPUT VOLTAGE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	REFOUT	+2.4	-	+2.6	V
VREFOUT Temperature Coefficient (Note 12)	$T_{VREFOUT}$	-	30	60	ppm/°C
Load Regulation (Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 12. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$T_{VREFOUT} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\cdot\left(\frac{1}{T_{A}{}_{MAX} - T_{A}{}_{MIN}}\right)\cdot\left(1.0 \times 10^{6}\right)$$

5V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, SCLK, and $\overline{\text{RESET}}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
High Impedance State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

13. Note that the 5 V characteristics are guaranteed by characterization. Only the more rigorous 3.3 V digital characteristics are actually verified during production test.

14. Applies to all INPUT pins except XIN pin (leakage current < 50 µA) and MODE pin (leakage current < 25 µA).

3.3 V DIGITAL CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5 V ±10%, VD+ = 3.3 V ±10%; VA-, DGND = 0 V) (See Notes 3, 4, and 13)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN, XOUT, SCLK, and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage (except XIN, XOUT) I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (except XIN, XOUT) I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 14)	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

Notes: 15. All measurements performed under static conditions.

16. If VD+ = 3 V and if XIN input is generated using crystal, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If using oscillator, full XIN frequency range is available, see *Switching Characteristics*.

ABSOLUTE MAXIMUM RATINGS

(DGND = 0 V; See Note 17) WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies (Notes 18 and 19)					
Positive Digital	VD+	-0.3	-	+6.0	V
Positive Analog	VA+	-0.3	-	+6.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies(Note 20, 21, and 22)	I_{IN}	-	-	±10	mA
Output Current	I_{OUT}	-	-	±25	mA
Power Dissipation (Note 23)	P_D	-	-	500	mW
Analog Input Voltage All Analog Pins	V_{INA}	(VA-) - 0.3	-	(VA+) + 0.3	V
Digital Input Voltage All Digital Pins	V_{IND}	DGND - 0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature	T_A	-40	-	85	°C
Storage Temperature	T_{stg}	-65	-	150	°C

Notes: 17. All voltages with respect to ground.

18. VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.0 V.
19. VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +6.0 V.
20. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.
21. Transient current of up to 100 mA will not cause SCR latch-up.
22. Maximum DC input current for a power supply pin is ±50 mA.
23. Total power dissipation, including all input currents and output currents.

SWITCHING CHARACTERISTICS

(T_A = -40 °C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50 pF))

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency Crystal/Internal Gate Oscillator (Note 24)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 25)		40		60	%
Rise Times Any Digital Input Except SCLK (Note 26)	t_{rise}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Fall Times Any Digital Input Except SCLK (Note 26)	t_{fall}	-	-	1.0	µs
SCLK		-	-	100	µs
Any Digital Output		-	50	-	ns
Start-up					
Oscillator Start-Up Time XTAL = 4.096 MHz (Note 27)	t_{ost}	-	60	-	ms
Serial Port Timing					
Serial Clock Frequency	SCLK	-	-	2	MHz
Serial Clock Pulse Width High	t_1	200	-	-	ns
Pulse Width Low	t_2	200	-	-	ns
SDI Timing					
CS Falling to SCLK Rising	t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising	t_4	50	-	-	ns
Data Hold Time After SCLK Rising	t_5	100	-	-	ns
SCLK Falling Prior to CS Disable	t_6	100	-	-	ns
SDO Timing					
CS Falling to SDI Driving	t_7	-	20	50	ns
SCLK Falling to New Data Bit	t_8	-	20	50	ns
CS Rising to SDO Hi-Z	t_9	-	20	50	ns
Auto-boot Timing					
Serial Clock Pulse Width High	t_{10}		8		MCLK
Pulse Width Low	t_{11}		8		MCLK
MODE setup time to RESET Rising	t_{12}	50			ns
RESET rising to CS falling	t_{13}	48			MCLK
CS falling to SCLK rising	t_{14}	100	8		MCLK
SCLK falling to CS rising	t_{15}		16		MCLK
CS rising to driving MODE low (to end auto-boot sequence).	t_{16}	50			ns
SDO guaranteed setup time to SCLK rising	t_{17}	100			ns

Notes: 24. Device parameters are specified with a 4.096 MHz clock, yet, clocks between 3 MHz to 20 MHz can be used. However, for input frequencies over 5 MHz, an external oscillator must be used.

25. If external MCLK is used, then duty cycle must be between 45% and 55% to maintain this specification.

26. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

27. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

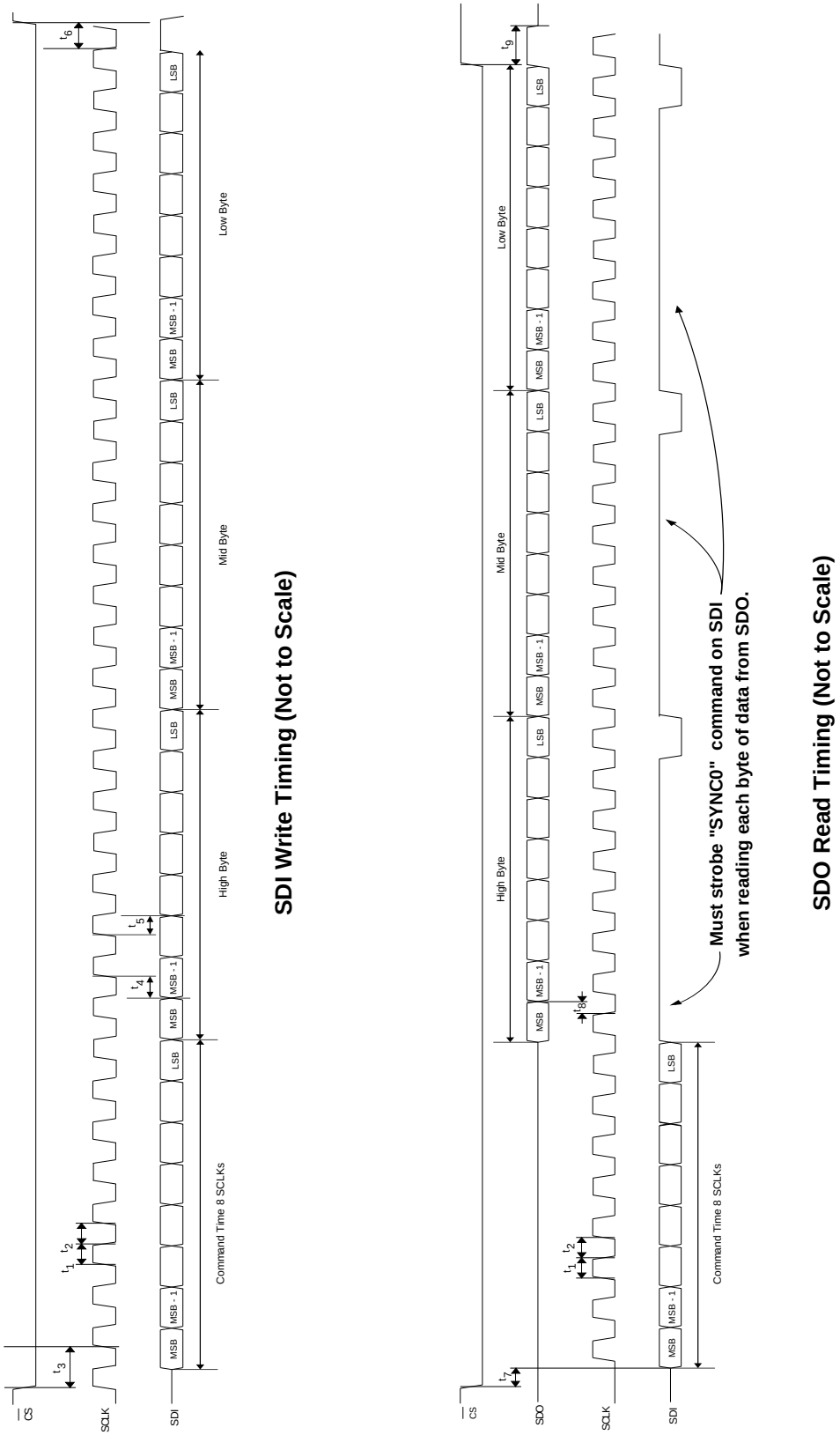


Figure 1. CS5460A Read and Write Timing Diagrams

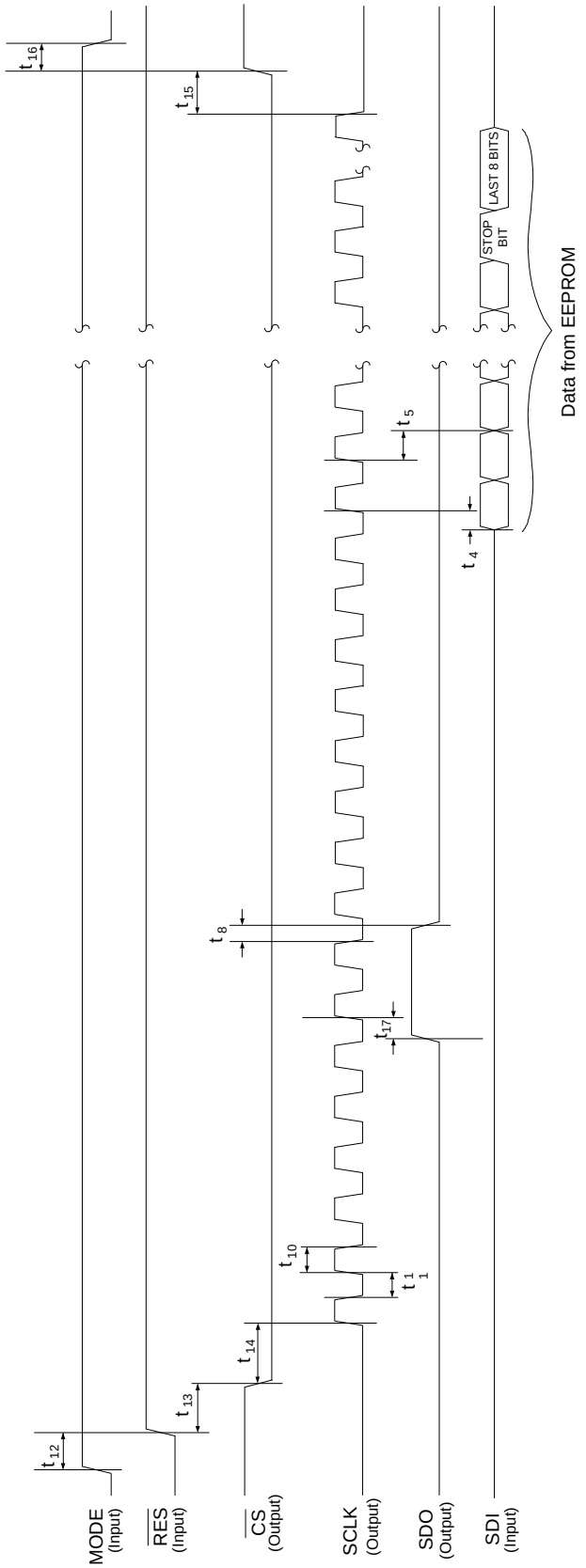


Figure 2. CS5460A Auto-boot Sequence Timing

2. OVERVIEW

The CS5460A is a CMOS monolithic power measurement device with a real power/energy computation engine. The CS5460A combines two programmable gain amplifiers, two ΔΣ modulators, two high rate filters, system calibration, and rms/power calculation functions to provide instantaneous voltage/current/power data samples as well as periodic computation results for real (billable) energy, V_{RMS}, and I_{RMS}. In order to accommodate lower cost metering applications, the CS5460A can also generate pulse-train signals on certain output pins, for which the number of pulses emitted on the pins is proportional to the quantity of real (billable) energy registered by the device.

The CS5460A is optimized for power measurement applications and is designed to interface to a shunt or current transformer to measure current, and to a resistive divider or potential transformer to measure voltage. To accommodate various input voltage levels, the current channel includes a programmable gain amplifier (PGA) which provides two full-scale input levels, while the voltage channel's PGA provides a single input voltage range. With a single +5 V supply on VA+/-, both of the CS5460A's input channels can accomodate common mode + signal levels between -0.25 V and VA+.

The CS5460A includes two high-rate digital filters (one per channel), which decimate/integrate the output from the 2 ΔΣ modulators. The filters yield 24-bit output data at a (MCLK/K)/1024 output word rate (OWR). The OWR can be thought of as the effective sample frequency of the voltage channel and the current channel.

To facilitate communication to a microcontroller, the CS5460A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The serial port has a Schmitt Trigger input on its SCLK (serial clock) and $\overline{\text{RESET}}$ pins to allow for slow rise time signals.

2.1 Theory of Operation

A computational flow diagram for the two data paths is shown in Fig. 3. The reader should refer to this diagram while reading the following data processing description, which is covered block-by-block.

2.1.1 ΔΣ Modulators

The analog waveforms at the voltage/current channel inputs are subject to the gains of the input PGAs (not shown in Figure 3). These waveforms are then sampled by the delta-sigma modulators at a rate of (MCLK/K)/8 Sps.

2.1.2 High-rate Digital Low-pass Filters

The data is then low-pass filtered, to remove high-frequency noise from the modulator output. Referring to Figure 3, the high rate filter on the voltage channel is implemented as a fixed $Sinc^2$ filter. The current channel uses a $Sinc^4$ filter, which allows the current channel to make accurate measurements over a wider span of the total input range, in comparison to the accuracy range of the voltage channel. (This subject is discussed more in *Section 2.2.1*)

Also note from Figure 3 that the digital data on the voltage channel is subjected to a variable time-delay filter. The amount of delay depends on the value of the seven phase compensation bits (see *Phase Compensation*). Note that when the phase compensation bits PC[6:0] are set to their default setting of "0000000" (and if MCLK/K = 4.096 MHz) then the nominal time delay that is imposed on the original analog voltage input signal, with respect to the original analog current input signal, is ~1.0 µs. This translates into a delay of ~0.0216 degrees at 60 Hz.

2.1.3 Digital Compensation Filters

The data from both channels is then passed through two FIR compensation filters, whose purpose is to compensate for the magnitude roll-off of the low-pass filtering operation (mentioned earlier).

2.1.4 Digital High-pass Filters

Both channels provide an optional high-pass filter (denoted as "HPF" in Figure 3) which can be engaged into the signal path, to remove the DC content from the current/voltage signal before the RMS/energy calculations are made. These filters are activated by enabling certain bits in the Configuration Register.

If the high-pass filter is engaged in only one of the two channels, then the all-pass filter (see "APF" in

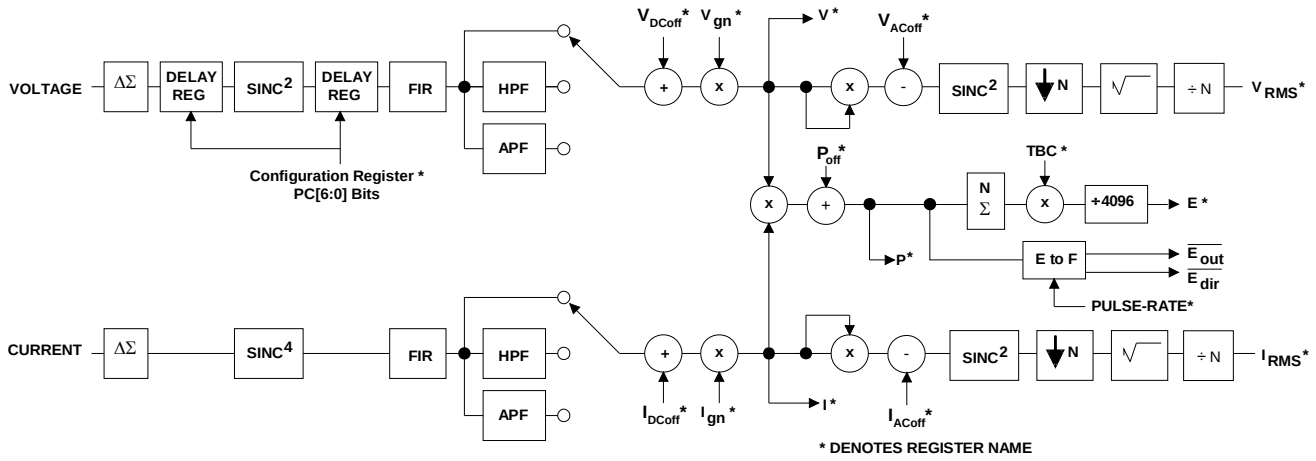


Figure 3. Data Flow.

Figure 3) will be enabled on the other channel; in order to preserve the relative phase relationship between the voltage-sense and current-sense input signals. For example, if the HPF is engaged for the voltage channel, but not the current channel, then the APF will be engaged in the current channel, to nullify the additional phase delay introduced by the high-pass filter in the current channel.

2.1.5 Overall Filter Response

When the CS5460A is driven with a 4.096 MHz clock (K = 1), the composite magnitude response (over frequency) of the voltage channel's input filter network is shown in Figure 4, while the composite magnitude response of the current channel's input filter network is given in Figure 5. Note that the composite filter response of both channels scales with MCLK frequency and K.

2.1.6 Gain and DC Offset Adjustment

After filtering, the instantaneous voltage and current digital codes are subjected to offset/gain adjustments, based on the values in the DC offset registers (additive) and the gain registers (multiplicative). These registers are used for calibration of the device (see *Section 3.8, Calibration*). After offset and gain, the 24-bit instantaneous data sample values are stored in the Instantaneous Voltage and Current Registers.

2.1.7 Real Energy and RMS Computations

The digital instantaneous voltage and current data is then processed further. Referring to Figure 3, the instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous (real) power samples. After each A/D conversion cycle, the new instantaneous power sample is stored in the Instantaneous Power Register.

The instantaneous power samples are then grouped into sets of N samples (where N = value in Cycle Count Register). The cumulative sum of each successive set of N instantaneous power is used to compute the result stored in the Energy Register, which will be proportional to the amount of real energy registered by the device during the most recent N A/D conversion cycles. Note from Figure 3 that the bits in this running energy sum are right-shifted 12 times (divided by 4096) to avoid overflow in the Energy Register. RMS calculations are also performed on the data using the last N instantaneous voltage/current samples, and these results can be read from the RMS Voltage Register and the RMS Current Register.

2.2 Performing Measurements

To summarize Section 2.1, the CS5460A performs measurements of instantaneous current and instantaneous voltage, and from this, performs computations of the corresponding instantaneous power, as well as periodic calculations of real energy, RMS current, and RMS voltage. These measurement/calculation results are available in the form of 24-bit signed and unsigned words. The scaling of all output words is normalized to unity

full-scale. Note that the 24-bit *signed* output words are expressed in two's complement format. The 24-bit data words in the CS5460A output registers represent values between 0 and 1 (for unsigned output registers) or between -1 and +1 (for signed output registers). A register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained in the registers of the CS5460A. As an illustration, in any of the signed output registers, the maximum register value is [(2^23 - 1) / (2^23)] = 0.999999880791. After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{\text{INT}}$ pin will also become active if the CRDY bit is unmasked (in the Mask Register). The assertion of the CRDY bit indicates that new instantaneous 24-bit voltage and current samples have been collected, and these two samples have also been multiplied together to provide a corresponding instantaneous 24-bit power sample.

Table 1 conveys the typical relationship between the differential input voltage (across the "+" and "-" input pins of the voltage channel input) and the corresponding output code in the Instantaneous Voltage Register. Note that this table is applicable for the current channel if the current channel's PGA gain is set for the "10x" gain mode.

Input Voltage (DC)	Output Code (hexidecimal)	Output Code (decimal)
+250 mV	7FFFFF	8388607
14.9 nV to 44.7 nV	000001	1
-14.9 nV to 14.9 nV	000000	0
-44.7 nV to -14.9 nV	FFFFFF	-1
-250 mV	800000	-8388608

Table 1. Differential Input Voltage vs. Output Code

The V_{RMS}, I_{RMS}, and energy calculations are updated every N conversions (which is known as 1 "*computation cycle*"), where N is the value in the Cycle Count Register. At the end of each computation cycle, the $\overline{\text{DRDY}}$ bit in the Mask Register will be set, and the $\overline{\text{INT}}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. Bits asserted by the CS5460A must be cleared before being asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the RMS results to be valid, the Cycle-Count Register must be set to a value greater than 10.

The computation cycle frequency is derived from the master clock, and has a value of (MCLK/K)/(1024*N). Under default conditions, with

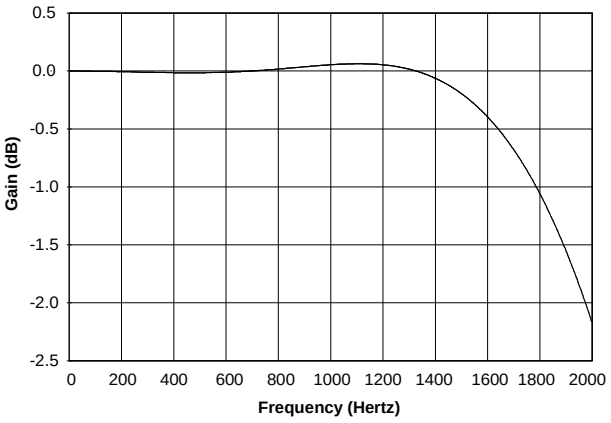


Figure 4. Voltage Input Filter Characteristics

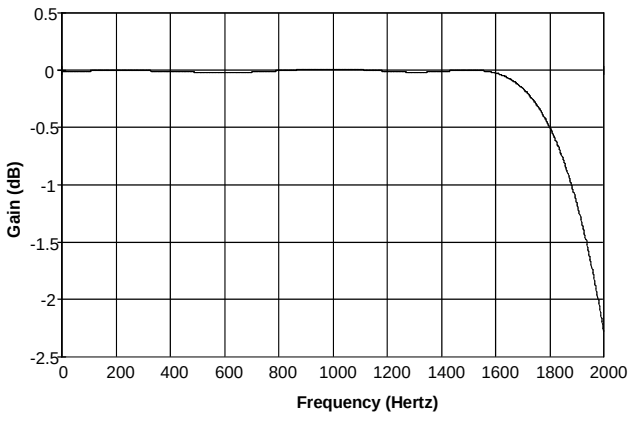


Figure 5. Current Input Filter Characteristics

a 4.096 MHz clock at XIN, and K = 1, instantaneous A/D conversions for voltage, current, and power are performed at a 4000 Sps rate, whereas I_{RMS}, V_{RMS}, and energy calculations are performed at a 1 Sps rate.

2.2.1 CS5460A Linearity Performance

Table 2 lists the range of input levels (as a percentage of full-scale) over which the (linearity + variation) of the results in the Vrms, Irms and Energy Registers are guaranteed to be within ±0.1 % of reading after the completion of each successive computation cycle. Note that until the CS5460A is calibrated (see Calibration) the *accuracy* of the CS5460A with respect to a reference line-voltage and line-current level on the power mains is not guaranteed to within ±0.1%. After both channels of the device are calibrated for offset/gain, the ±0.1% of reading spec will also reflect accuracy of the Vrms, Irms, and Energy Register results. Finally, observe that the maximum (full-scale) differential input voltage for the voltage channel (and current channel, when its PGA is set for 10x gain) is 250 mV (nominal). **If the gain registers of both channels are set to 1 (default) and the two DC offset registers are set to zero (default), then a 250mV DC signal applied to the voltage/current inputs will measure at (or near) the maximum value of 0.9999... in the RMS Current/Voltage Registers.** Remember that the RMS value of a 250 mV (DC) signal is also 250 mV. However, for either input channel, it would not be practical to inject a sinusoidal voltage with RMS value of 250 mV. This is because when the instantaneous value of such a sine wave is at or near the level of its positive/negative peak regions (over each cycle), the voltage level of this signal would exceed the maximum differential input voltage range of the input channels. The largest sine wave voltage signal that can be presented across the inputs, with no saturation of the inputs, is:

250 mV / sqrt(2) = ~176.78 mV (RMS),

which is ~70.7% of full-scale. This would imply that for the current channel, the (linearity+variation) tolerance of the RMS measurements for a purely sinusoidal 60 Hz input signal could be measured to within ±0.1% of reading over a magnitude range of 0.2% - 70.7% of the maximum full-scale differential input voltage level.

The range over which the (linearity + variation) will remain within ±0.1% can often be increased by selecting a value for the Cycle-Count Register such that the time duration of one computation cycle is equal to (or very close to) a *whole-number* of power-line cycles (and N must be greater than or equal to 4000). For example, with the cycle count set to 4200, the ±0.1% of reading (linearity + variation) range for measurement of a 60 Hz sinusoidal current-sense voltage signal can be increased beyond the range of 0.2% - 70.7%. The accuracy range will be increased because (4200 samples / 60 Hz) is a whole number of cycles (70). Note that this increase in the measurement range refers to an extension of the *low* end of the input scale (i.e., this does *not* extend the high-end of the range above 100% of full-scale). This enables accurate measurement of even smaller power-line current levels, thereby extending the load range over which the power meter can make accurate energy measurements. Increasing the accuracy range can be beneficial for power metering applications which require accurate power metering over a very large load range.

	Energy	Vrms	Irms
Range (% of FS)	0.1% - 100%	50% - 100%	0.2% - 100%
Max. Differential Input	*not applicable*	V-channel: ±250 mV	I-channel: ±250 mV 10x ±50 mV 50x
Linearity	0.1% of reading	0.1% of reading	0.1% of reading

Table 2. Available range of ±0.1% output linearity, with default settings in the gain/offset registers.

2.2.2 Single Computation Cycle (C=0)

Note that 'C' refers to the value of the C bit, contained in the 'Start Conversions' command (see Section 4.1). This commands instructs the CS5460A to perform conversions in 'single computation cycle' data acquisition mode. Based on the value in the Cycle Count Register, a single computation cycle is performed after a 'Start Conversions' command is sent to the serial interface. After the computations are complete, DRDY is set. 32 SCLKs are then needed to read out a calculation

result from one of several result registers. The first 8 SCLKs are used to clock in the command to determine which register is to be read. The last 24 SCLKs are used to read the desired register. After reading the data, the serial port remains in the *active state*, and waits for a new command to be issued. (See Section 3 for more details on reading register data from the CS5460A).

2.2.3 Continuous Computation Cycles (C=1)

When C = 1, the CS5460A will perform conversions in 'continuous computation cycles' data acquisition mode. Based on the information provided in the Cycle Count Register, computation cycles are repeatedly performed on the voltage and current channels (after every N conversions). Computation cycles cannot be started/stopped on a 'per-channel' basis. After each computation cycle is completed, DRDY is set. Thirty-two SCLKs are then needed to read a register. The first 8 SCLKs are used to clock in the command to determine which results register is to be read. The last 24 SCLKs are used to read out the 24-bit calculation result. While in this acquisition mode, the designer/programmer may choose to acquire (read) only those calculations required for their particular application, as DRDY repeatedly indicates the availability of new data. Note again that the MCU firmware must reset the DRDY bit to "0" before it can be asserted again.

Referring again to Figure 3, note that within the Irms and Vrms data paths, prior to the square-root operation, the instantaneous voltage/current data is low-pass filtered by a $Sinc^2$ filter. Then the data is decimated to every Nth sample. Because of the $Sinc^2$ filter operation, the first output for each channel will be invalid (i.e. all RMS calculations are invalid in the 'single computation cycle' data acquisition mode and the first RMS calculation results will be invalid in the 'continuous computation cycles' data acquisition mode). However, all energy calculations will be valid since energy calculations do not require this $Sinc^2$ operation.

If the 'Start Conversions' command is issued to the CS5460A (see *Section 4.1, Commands (Write Only)*), and if the 'C' bit in this command is set to a value of '1', the device will remain in its *active state*. Once commanded into *continuous computation cycles* data acquisition mode, the CS5460A will continue to perform A/D conversions on the voltage/current channels, as well as all subsequent calculations, until:

1) the 'Power-Up/Halt' command is received through the serial interface, or
2) loss of power, or
3) the RS bit in the Configuration Register is asserted ('software reset'), or
4) the /RESET pin is asserted and then de-asserted ('hardware reset').

2.3 Basic Application Circuit Configurations

Figure 6 shows the CS5460A connected to a service to measure power in a single-phase 2-wire system operating from a single power supply. Note that in this diagram the shunt resistor used to monitor the line current is connected on the "Line" (hot) side of the power mains. In most residential power metering applications, the power meter's current-sense shunt resistor is intentionally placed on the 'hot' side of the power mains in order to help detect any attempt by the subscriber to steal power. In this type of shunt-resistor configuration, note that the common-mode level of the CS5460A must be referenced to the hot side of the power line. This means that the common-mode potential of the CS5460A will typically oscillate to very high positive voltage levels, as well as very high negative voltage levels, with respect to earth ground potential. *The designer must therefore be careful* when attempting to interface the CS5460A's digital output lines to an external digital interface (such as a LAN connection or other communication network). Such digital communication networks may require that the CMOS-level digital interface to the meter is referenced to an earth-ground. In such cases, the CS5460A's digital serial interface pins *must be isolated* from the external digital interface, so that there is no conflict between the ground references of the meter and the external interface. The CS5460A and associate circuitry should be enclosed in a protective insulated case when used in this configuration, to avoid risk of harmful electric shock to humans/animals/etc.

Figure 7 shows how the same single-phase two-wire system can be metered while achieving

complete isolation from the power lines. This isolation is achieved using three transformers. One transformer is a general-purpose voltage transformer, used to supply the on-board DC power to the CS5460A. A second transformer is a high-precision, low-impedance voltage transformer (often called a 'potential transformer') with very little roll-off/phase delay, even at the higher harmonics. A current transformer is then used to sense the line current. A burden resistor placed across the secondary of the current transformer creates the current-sense voltage signal, for the CS5460A's current channel inputs. Because the CS5460A is not directly connected to the power mains, isolation is not required for the CS5460A's digital interface.

Figure 8 shows the CS5460A configured to measure power in a single-phase 3-wire system. In many 3-wire residential power systems within the United States, only the two Line terminals are available (neutral is not available). Figure 9 shows how the CS5460A can be configured to meter a 3-wire system when no neutral is available.

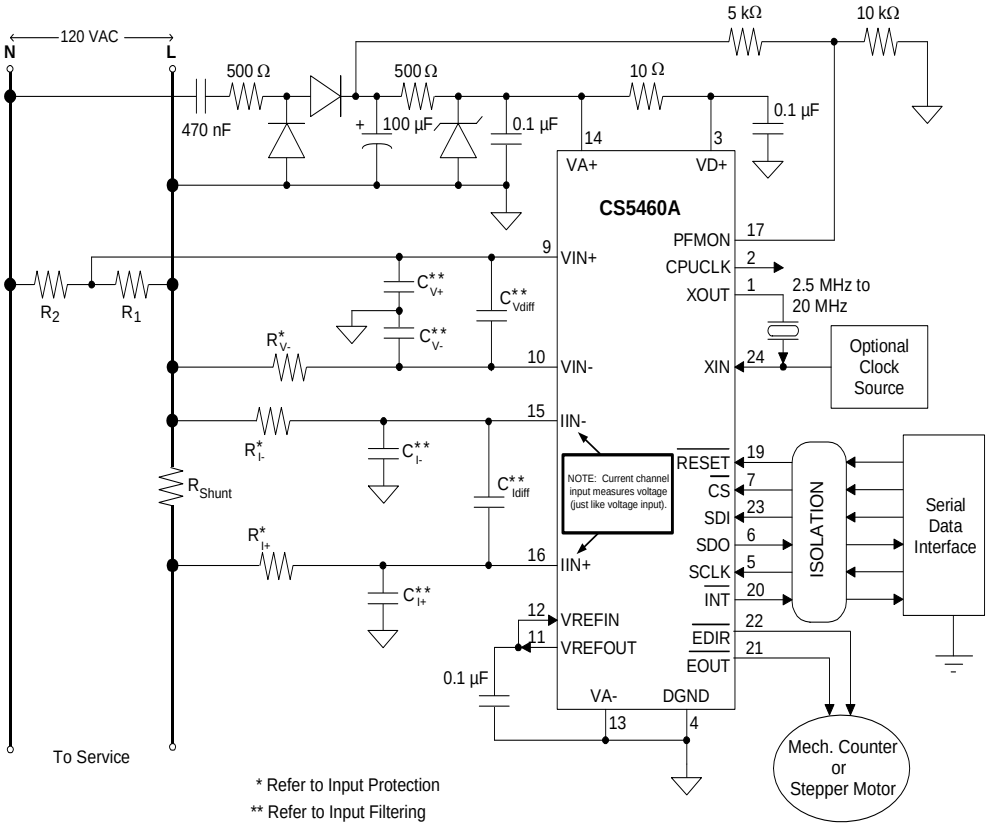


Figure 6. Typical Connection Diagram (One-Phase 2-Wire, Direct Connect to Power Line)

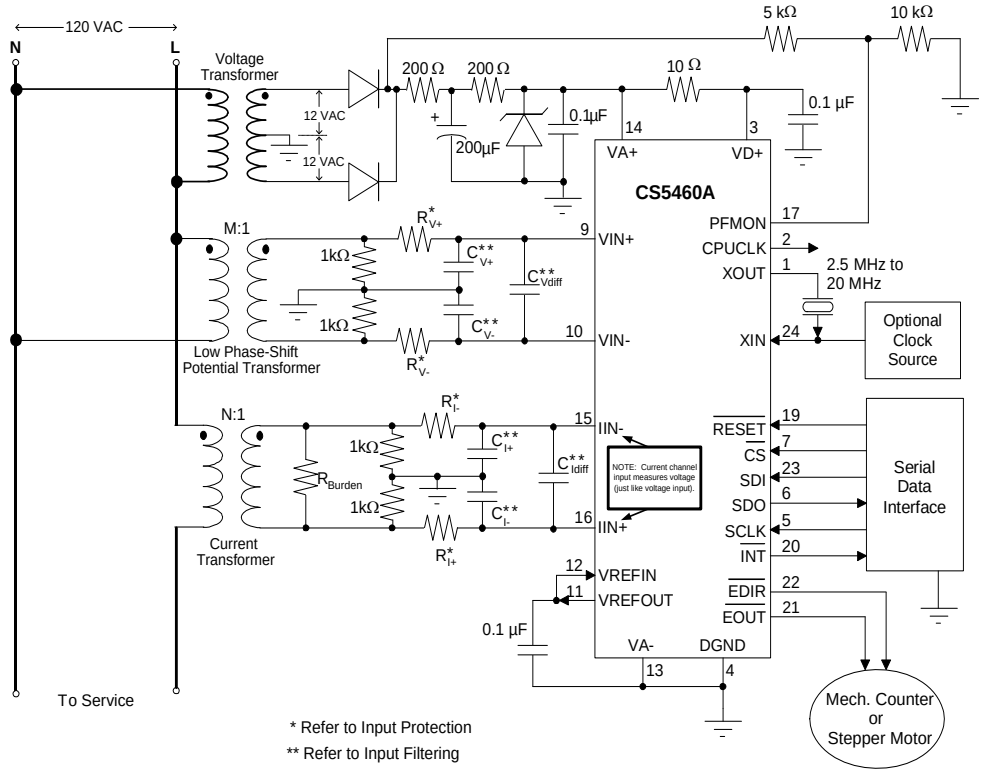


Figure 7. Typical Connection Diagram (One-Phase 2-Wire, Isolated from Power Line)

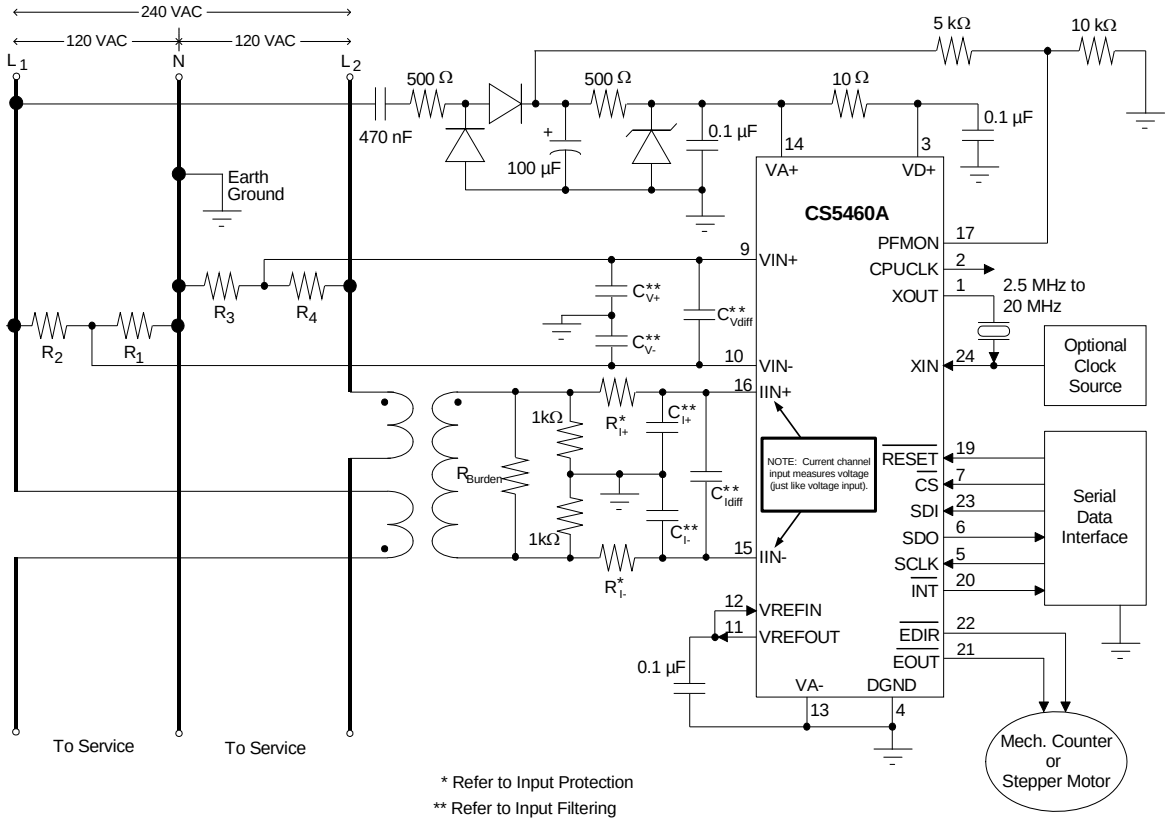


Figure 8. Typical Connection Diagram (One-Phase 3-Wire)

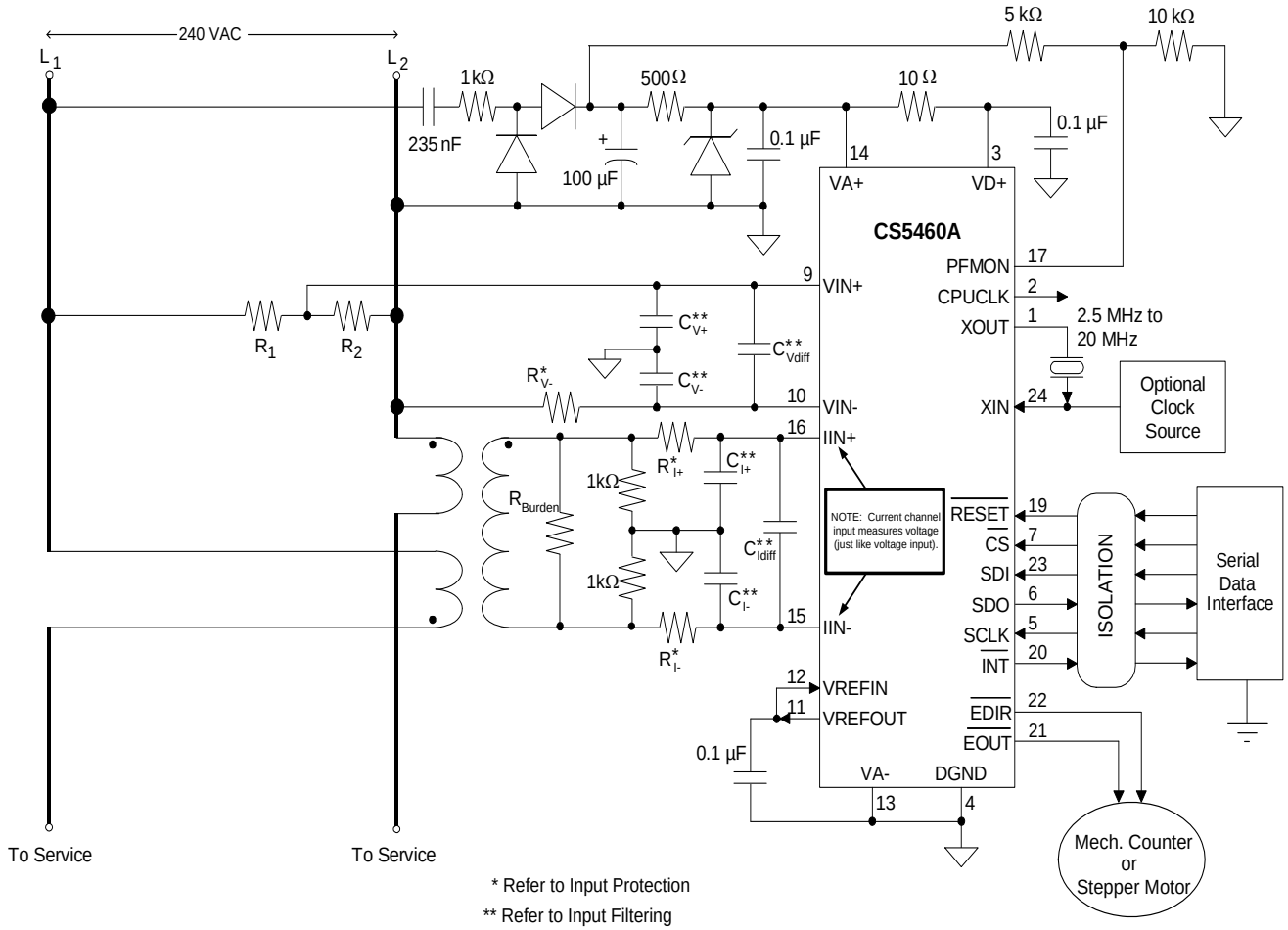


Figure 9. Typical Connection Diagram (One-Phase 3-Wire - No Neutral Available)

3. FUNCTIONAL DESCRIPTION

3.1 Pulse-Rate Output

As an alternative to reading the real energy through the serial port, the EOUT and EDIR pins provide a simple interface with which signed energy can be accumulated. Each EOUT pulse represents a predetermined quantity of energy. The quantity of energy represented in one pulse can be varied by adjusting the value in the Pulse-Rate Register. Corresponding pulses on the EDIR output pin signify that the sign of the energy is negative. Note that these pulses are not influenced by the value of the Cycle-Count Register, and they have no reliance on the computation cycle, described earlier. With MCLK = 4.096 MHz, K = 1, the pulses will have an average frequency (in Hz) equal to the frequency setting in the Pulse Rate Register when the input signals into the voltage and current channels cause full-scale readings in the Instantaneous Voltage and Current Registers. When MCLK/K is not equal to 4.096 MHz, the pulse-rate should be scaled by a factor of 4.096 MHz / (MCLK/K) to get the actual output pulse-rate.

EXAMPLE #1: For a power line with maximum rated levels of 250 V (RMS) and 20 A (RMS), the pulse-frequency on the EOUT pin needs to be 'IR' = 100 pulses-per-second (100 Hz) when the RMS-voltage and RMS-current levels on the power line are 220 V and 15 A respectively. To meet this requirement, the pulse-rate frequency ('PR') in the Pulse-Rate Register must be set accordingly.

After calibration, the first step to finding the value of 'PR' is to set the voltage and current sensor gain constants, K_V and K_I, such that there will be acceptable voltage levels on the CS5460A inputs when the power line voltage and current levels are at the maximum values of 250 V and 20 A. K_V and K_I are needed to determine the appropriate ratios of the voltage/current transformers and/or shunt resistor values to use in the front-end voltage/current sensor networks.

For a sinewave, the largest RMS value that can be accurately measured (without over-driving the inputs) will register ~0.7071 of the maximum DC input level. Since power signals are often not perfectly sinusoidal in real-world situations, and to provide for some over-range capability, the RMS Voltage Register and RMS Current Register is set to measure 0.6 when the RMS-values of the line-voltage and line-current levels are 250 V and 20 A. Therefore, when the RMS registers measure 0.6, the voltage level at the inputs will be 0.6 x 250 mV = 150 mV. The sensor gain constants, K_V and K_I, are determined by demanding that the voltage and current channel inputs should be 150 mV RMS when the power line voltage and current are at the maximum values of 250 V and 20 A.

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

These sensor gain constants are used to calculate what the input voltage levels will be on the CS5460A inputs when the line-voltage and line-current are 220 V and 15 A. These values are V_{Vnom} and V_{Inom}.

$V_{Vnom} = K_V * 220\ V = 132\ mV$

$V_{Inom} = K_I * 15\ A = 112.5\ mV$

The pulse rate on EOUT will be at 'PR' pulses per second (Hz) when the RMS-levels of voltage/current inputs are at 250 mV. When the voltage/current inputs are set at V_{Vnom} and V_{Inom}, the pulse rate needs to be 'IR' = 100 pulses per second. IR will be some percentage of PR. The percentage is defined by the ratios of V_{Vnom}/250 mV and V_{Inom}/250 mV with the following formula:

$$\text{PulseRate} = IR = PR \cdot \frac{V_{Vnom}}{250mV} \cdot \frac{V_{Inom}}{250mV}$$

From this equation the value of 'PR' is shown as:.

$$PR = \frac{IR}{\frac{V_{Vnom}}{250mV} \times \frac{V_{Inom}}{250mV}} = \frac{100Hz}{\frac{132mV}{250mV} \times \frac{112.5mV}{250mV}}$$

Therefore the Pulse-Rate Register is set to ~420.875 Hz, or 0x00349C.

The above equation is valid when current channel is set to x10 gain. If current channel gain is set to x50, then the equation becomes:

$$PR = \frac{IR}{\frac{V_{Vnom}}{250mV} \times \frac{V_{Inom}}{50mV}}$$

EXAMPLE #2: The required number of pulses per unit energy present at EOUT is specified to be 500 pulses/kW-hr; given that the maximum line-voltage is 250 V (RMS) and the maximum line-current is 20 A (RMS). In such a situation, the nominal line voltage and current do not determine the appropriate pulse-rate setting. Instead, the maximum line levels must be considered. As before, the given maximum line-voltage and line-current levels are used to determine K_V and K_I:

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ω

Again the sensor gains are calculated such that the maximum line-voltage and line-current levels will measure as 0.6 in the RMS Voltage Register and RMS Current Register.

The required Pulse-Rate Register setting is now determined by using the following equation:

$$PR = 500\frac{pulses}{kW \cdot hr} \cdot \frac{1hr}{3600s} \cdot \frac{1kW}{1000W} \cdot \frac{250mV}{K_V} \cdot \frac{250mV}{K_I}$$

Therefore PR = ~1.929 Hz.

Note that the Pulse-Rate Register cannot be set to a frequency of exactly 1.929 Hz. The closest setting that the Pulse-Rate Register can obtain is 0x00003E = 1.9375 Hz. To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$Ign \text{ or } Vgn = \frac{PR}{1.929} \cong 1.00441 = 0x404830$$

In the last example, suppose a value for MCLK/K of 3.05856 MHz. When MCLK/K is not equal to 4.096 MHz, the result for 'PR' that is calculated for the Pulse-Rate Register must be scaled by a correction factor of: 4.096 MHz / (MCLK/K). In this case the result is scaled by 4.096/3.05856 to get a final PR result of ~2.583 Hz.

3.2 Pulse Output for Normal Format, Stepper Motor Format and Mechanical Counter Format

The duration and shape of the pulse outputs at the EOUT and EDIR pins can be set for three different output formats. The default setting is for *Normal* output pulse format. When the pulse is set to either of the other two formats, the time duration and/or the relative timing of the EOUT and EDIR pulses is increased/varied such that the pulses can drive either an electro-mechanical counter or a stepper motor. The EOUT and EDIR output pins are capable of driving certain low-voltage/low-power counters/stepper motors directly. This depends on the drive current and voltage level requirements of the counter/motor. The ability to set the pulse output format to one of the three available formats is controlled by setting certain bits in the Control Register.

3.2.1 Normal Format

Referring to the description of the Control Register in *Section 5., Register Descriptions*, if both the MECH and STEP bits are set to '0', the pulse output format at the EOUT and EDIR pins is illustrated in Figure 10. These are active-low pulses with very short duration. The pulse duration is an integer multiple of MCLK cycles, approximately equal to 1/16 of the period of the contents of the Pulse-Rate Register. However for Pulse-Rate Register settings less than the sampling rate (which is [MCLK/8]/1024), the pulse duration will remain at a constant duration, which is equal to the duration of the pulses when the Pulse-Rate Register is set to [MCLK/K]/1024. The maximum pulse frequency from the EOUT pin is therefore [MCLK/K]/16. When energy is positive, EDIR is always high. When energy is negative, EDIR has the same output as EOUT. When MCLK/K is not equal to 4.096 MHz, the true pulse-rate can be found by first calculating what the pulse-rate would be if a 4.096 MHz crystal is used (with K = 1) and then scaling the result by a factor of (MCLK/K) / 4.096 MHz.

When set to run in *Normal* pulse output format, the pulses may be sent out in "bursts" depending on both the value of the Pulse-Rate Register as well as the amount of billable energy that was registered by the CS5460A over the most recent A/D sampling period, which is (in Hz): 1 / [(MCLK/K) / 1024]. A running total of the energy accumulation is maintained in an internal register (not accessible to the user) inside the CS5460A. If the amount of energy that has accumulated in this register over the most recent A/D sampling period is equal to or greater than the amount of energy that is repre-

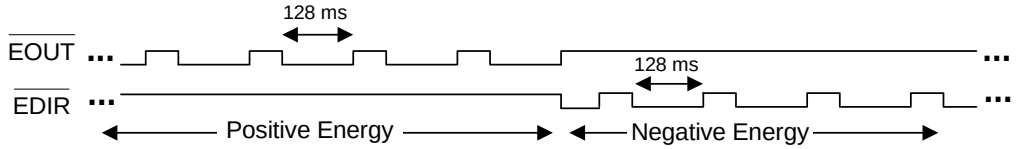


Figure 11. Mechanical Counter Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

sented by one pulse, the CS5460A will issue a "burst" of one or more pulses on $\overline{\text{EOUT}}$ (and also possibly on $\overline{\text{EDIR}}$). The CS5460A will issue as many pulses as are necessary to reduce the running energy accumulation value in this register to a value that is less than the energy represented in one pulse. If the amount of energy that has been registered over the most recent sampling period is large enough that it cannot be expressed with only one pulse, then a burst of pulses will be issued, possibly followed by a period of time during which there will be no pulses, until the next A/D sampling period occurs. After the pulse or pulses are issued, a certain residual amount of energy may be left over in this internal energy accumulation register, which is always less (in magnitude) than the amount of energy represented by one pulse. In this situation, the residual energy is not lost or discarded, but rather it is maintained and added to the energy that is accumulated during the next A/D conversion cycle. The amount of residual energy that can be left over becomes larger as the Pulse-Rate Register is set to lower and lower values, because lower Pulse-Rate Register values correspond to a higher amount of energy per pulse (for a given calibration).

3.2.2 Mechanical Counter Format

Setting the MECH bit in the Control Register to '1' and the STEP bit to '0' enables wide-stepping pulses for mechanical counters and similar discrete counter instruments. In this format, active-low pulses are 128 ms wide when using a 4.096 MHz crystal and K = 1. When energy is positive, the pulses appear on $\overline{\text{EOUT}}$. When energy is negative, pulses appear on $\overline{\text{EDIR}}$. To insure that pulses will not occur at a rate faster than the 128 ms pulse duration, or faster than the mechanical counter can accommodate, the Pulse-Rate Register should be set to an appropriate value. Because the duration of each pulse is set to 128 ms, the maximum output pulse frequency is limited to ~7.8 Hz (for MCLK/K = 4.096 MHz). For values of MCLK / K different than 4.096 MHz, the duration of one pulse is (128 * 4.096 MHz) / (MCLK / K) milliseconds. See Figure 11 for a diagram of the typical pulse output.

3.2.3 Stepper Motor Format

Setting the STEP bit in the Control Register to '1' and the MECH bit to '0' transforms the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins into two stepper motor phase outputs. When enough energy has been registered by the CS5460A to register one positive/negative energy

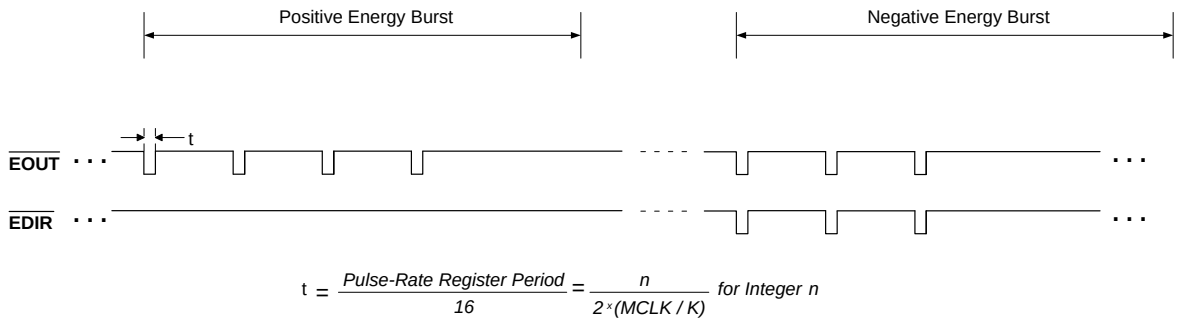


Figure 10. Time-plot representation of pulse output for a typical burst of pulses (Normal Format)

pulse, one of the output pins (either EOUT or EDIR) changes state. When the CS5460A must issue another energy pulse, the other output changes state. The direction the motor will rotate is determined by the order of the state changes. When energy is positive, EOUT will lead EDIR such that the EOUT pulse train will lead the EDIR pulse train by ~1/4 of the periods of these two pulse train signal. When energy is negative, EDIR will lead EOUT in a similar manner. See Figure 12.

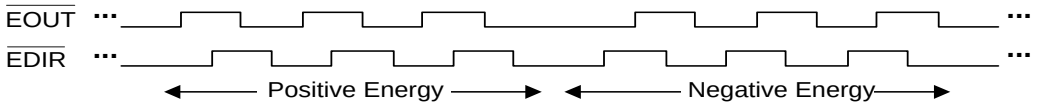


Figure 12. Stepper Motor Format on EOUT and EDIR

3.3 Auto-boot Mode Using EEPROM

The CS5460A has a MODE pin. When the MODE pin is set to logic low, the CS5460A is in normal operating mode, called *host mode*. This mode denotes the normal operation of the part, that has been described so far. But when this pin is set to logic high, the CS5460A *auto-boot mode* is enabled. In auto-boot mode, the CS5460A is configured to request a memory download from an external serial EEPROM. The download sequence is initiated by driving the RESET pin to logic high. Auto-boot mode allows the CS5460A to operate without the need for a microcontroller. Note that if the MODE pin is left unconnected, it will default to logic low because of an internal pull-down on the pin.

3.3.1 Auto-boot Configuration

Figure 13 shows the typical connections between the CS5460A and a serial EEPROM for proper auto-boot operation. In this mode, CS and SCLK are driven outputs. SDO is always an output. During the auto-boot sequence, the CS5460A drives CS low, provides a clock output on SCLK, and drives out-commands on SDO. It receives the EEPROM data on SDI. The serial EEPROM must be programmed with the user-specified commands and register data that will be used by the CS5460A to change any of the default register values (if desired) and begin conversions.

Figure 13 also shows the external connections that would be made to a calibrator device, such as a PC

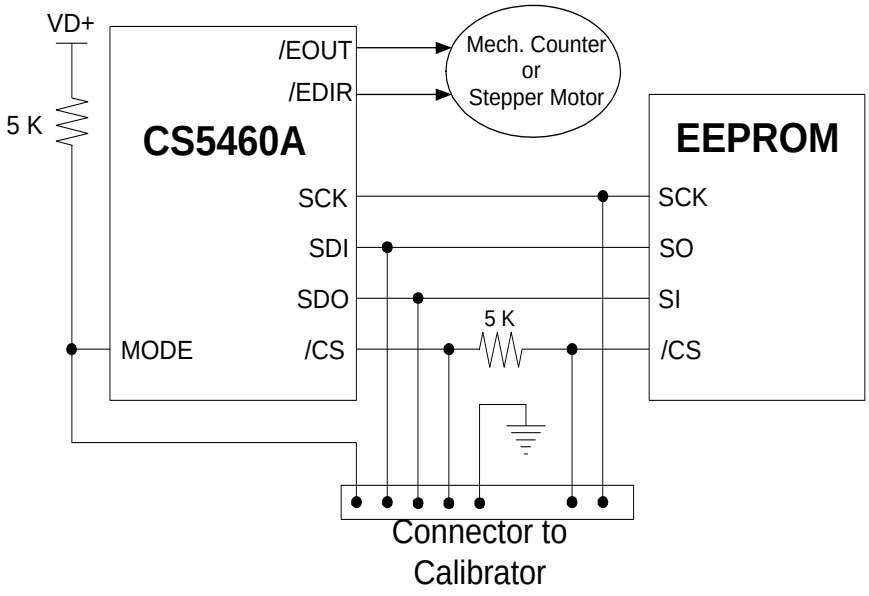


Figure 13. Typical Interface of EEPROM to CS5460A

or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the EEPROM. The commands/data will determine the CS5460A's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

3.3.2 Auto-boot Data for EEPROM

This section illustrates what a typical set of code would look like for an auto-boot sequence. This code is what would be written into the EEPROM. In the sequence below, the EEPROM is programmed so that it will first send out commands that write calibration values to the calibration registers inside the CS5460A. This is followed by the commands used to set (write) the desired Pulse-Rate Register value, and also to un-mask the 'LSD' status bit in the Mask Register. Finally, the EEPROM code will initiate 'continuous computation cycles' data acquisition mode and select one of the alternate pulse-output formats (e.g., set the MECH bit in the Control Register). The serial data for such a sequence is shown below in single-byte hexidecimal notation:

40 00 00 61	;Write to Configuration Register, turn high-pass filters on, set K = 1.
44 7F C4 A9	;Write value of 0x7FC4A9 to Current Channel Gain Register.
46 7F B2 53	;Write value of 0x7FB253 to Voltage Channel DC Offset Register.
4C 00 00 14	;Set Pulse Rate Register to 0.625 Hz.
74 00 00 04	;Unmask bit #2 ("LSD" bit in the Mask Register).
E8	;Start performing continuous computation cycles.
78 00 01 40	;Write STOP bit to Control Register, to terminate auto-boot initialization sequence, and also set the EOUT pulse output to Mechanical Counter Format.

This data from the EEPROM will drive the SDI pin of the CS5460A during the auto-boot sequence.

The following sequence of events will cause the CS5460A to execute the auto-boot mode initialization sequence: (A simple timing diagram for this sequence is shown below in Figure 14.) If the MODE pin is set to logic high (or if the MODE pin was set/tied to logic high during/after the CS5460A has been powered on), then changing the RESET pin from active state to inactive state (low to high) will cause the CS5460A to drive the CS pin low, and after this, to issue the standard EEPROM block-read command on the CS5460A's SDO line. Once these events have completed, the CS5460A will continue to issue SCLK pulses, to accept data/commands from the EEPROM. The serial port will become a *master*-mode interface. For a more detailed timing diagram, see *Switching Characteristics* (in *Section 1*.)

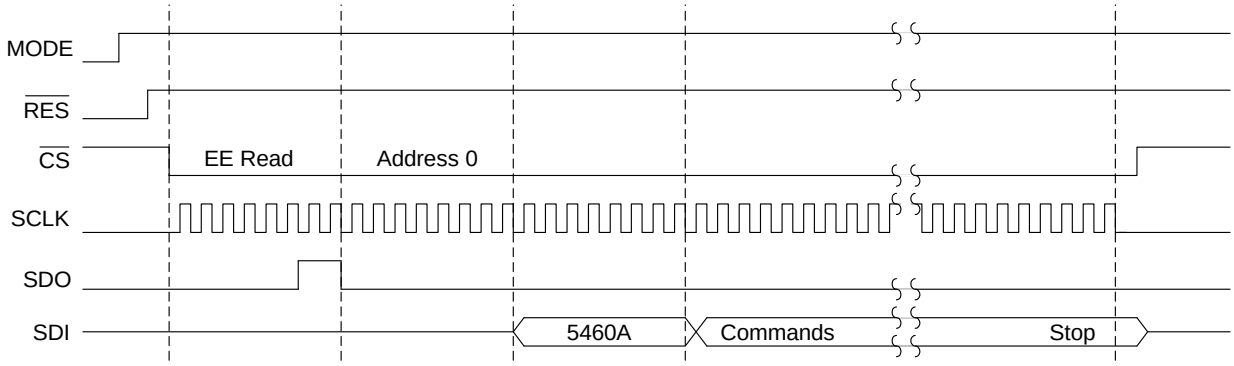


Figure 14. Timing Diagram for Auto-boot Sequence

3.3.3 Application Note AN225

For more information on Auto-boot mode, see the *AN225*, “USING THE CS5460A AUTO-BOOT MODE”.

3.4 Interrupt and Watchdog Timer

3.4.1 Interrupt

The $\overline{\text{INT}}$ pin is used to indicate that an event has taken place in the CS5460A that (may) need attention. These events inform the meter system about operation conditions and internal error conditions. The $\overline{\text{INT}}$ signal is created by combining the Status Register with the Mask Register. Whenever a bit in the Status Register becomes active, and the corresponding bit in the Mask Register is a logic 1, the $\overline{\text{INT}}$ signal becomes active.

3.4.1.1 Clearing the Status Register

Unlike the other registers, the bits in the Status Register can only be cleared (set to logic 0). When a word is written to the Status Register, any 1s in the word will cause the corresponding bits in the Status Register to be cleared. The other bits of the Status Register remain unchanged. This allows the clearing of particular bits in the register without having to know the state of the other bits. This mechanism is designed to facilitate handshaking and to minimize the risk of losing events that haven’t been processed yet.

3.4.1.2 Typical use of the $\overline{\text{INT}}$ pin

The steps below show how interrupts can be handled by the on-board MCU.

- *Initialization*:

  Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status Register.

  Step I1 - The conditional bits which will be used to generate interrupts are then written to logic 1 in the Mask Register.

  Step I2 - Enable interrupts.

- *Interrupt Handler Routine*:

  Step H0 - Read the Status Register.

  Step H1 - Disable all interrupts.

  Step H2 - Branch to the proper interrupt service routine.

  Step H3 - Clear the Status Register by writing back the value read in step H0.

  Step H4 - Re-enable interrupts.

  Step H5 - Return from interrupt service routine.

  This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

3.4.1.3 $\overline{\text{INT}}$ Active State

The behavior of the $\overline{\text{INT}}$ pin is controlled by the SI1 and SI0 bits of the Configuration Register. The pin can be active low (default), active high, active on a return to logic 0 (pulse-low), or active on a return to logic 1 (pulse-high).

If the interrupt output signal format is set for either active-high or active-low assertion, the interrupt condition is cleared when the bits of the Status Register are returned to their inactive state. If the interrupt output signal format is set for either pulse-high or pulse-low, note that the duration of the $\overline{\text{INT}}$ pulse will be at least one MCLK/K cycle, although in some cases the pulse may last for 2 MCLK/K cycles.

3.4.1.4 Exceptions

The $\overline{\text{IC}}$ (Invalid Command) bit of the Status Register can only be cleared by performing the port initialization sequence. This is also the only Status Register bit that is active low.

To properly clear the WDT (Watch Dog Timer) bit of the Status Register, first read the Energy Register, then clear the bit in the Status Register.

3.4.2 Watch Dog Timer

The Watch Dog Timer (WDT) is provided as a means of alerting the system that there is a potential breakdown in communication with the microcontroller. By allowing the WDT to cause an interrupt, a controller can be brought back, from some unknown code space, into the proper code for processing the data created by the converter. The time-out is preprogrammed to approximately 5 seconds. The countdown restarts each time the Energy Register is read. Under typical situations, the Energy Register is read every second. As a result, the WDT will not time out. Other applications that use the watchdog timer will need to ensure

that the Energy Register is read at least once in every 5 second span.

3.5 Oscillator Characteristics

XIN and XOUT are the input and output, respectively, of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 15. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 are integrated in the device, one between XIN and DGND, one between XOUT and DGND. Lead lengths should be minimized to reduce stray capacitance.

To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5460A can be driven by a clock ranging from 2.5 to 20 MHz. The K divider must be set to the appropriate value such that MCLK/K will be between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the Configuration Register. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then MCLK/K = 3 MHz, which is a valid value for MCLK/K. Note that if the K[3:0] bits are all set to zero, the value of the K divider value is 16.

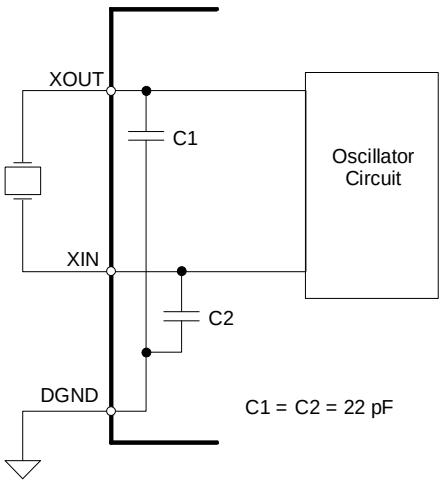


Figure 15. Oscillator Connection

3.6 Analog Inputs

The CS5460A accommodates a full-scale differential input voltage range of ±250 mV on both input channels. (If the PGA setting on the current channel is set for the 50x gain setting instead of the 10x gain setting, then the differential full-scale input range on the current channel reduces to ±50 mV.) System calibration can be used to increase or decrease the full scale span of the converter as long as the calibration register values stay within the limits specified. See *Section 3.8, Calibration*, for more details.

3.7 Voltage Reference

The CS5460A is specified for operation with a +2.5 V reference between the VREFIN and VA- pins. A reference voltage *must* be supplied to the VREFIN pin for proper operation of the two ADCs.

The CS5460A includes an internal 2.5 V reference, available on the VREFOUT pin, that can be used as the reference input voltage by connecting the VREFOUT pin to the VREFIN pin. If lower temperature drift is desired, an external reference can be used; in which case the VREFOUT pin should be left unconnected.

3.8 Calibration

3.8.1 Overview of Calibration Process

The CS5460A offers digital calibration. Each calibration sequence will be executed by setting/clearing one or more of the 8 bits in the *calibration command* word. For both channels, there are calibration sequences for both AC and DC purposes. Regardless of whether an AC or DC calibration sequence is desired, there are two basic types of calibrations: system offset and system gain. During the calibration sequences, proper input calibration signals to the “+” and “-” pins of the voltage-/current-channel inputs must be supplied. These input calibration signals represent full-scale levels (for gain calibrations) and ground input levels (for offset calibrations).

The AC and DC calibration sequences are different. Depending on the specific metering application and accuracy requirements, some or all of the calibration sequences may not be executed. (This

is explained in more detail in the following paragraphs).

3.8.2 The Calibration Registers

Refer to Figure 3 and Figure 21.

Voltage Channel DC Offset Register and Current Channel DC Offset Register - Store additive correction values that are used to correct for DC offsets which may be present on the voltage/current channels within the entire meter system. These registers are updated by the CS5460A after a DC offset calibration sequence has been executed.

Voltage Channel Gain Register and Current Channel Gain Register - Store the multiplicative correction values determined by the full-scale gain calibration signals that are applied to the meter's voltage/current channels. These registers are updated by the CS5460A after either an AC or DC gain calibration sequence has been executed.

Voltage Channel AC Offset Register and Current Channel AC Offset Register - Store additive offset correction values that are used to correct for AC offsets which may be created on the voltage/current channels within the entire meter system. Although a noise signal may have an average value of zero [no DC offset] the noise may still have a non-zero rms value, which can add an undesirable offset in the CS5460A's Irms and Vrms results. These registers are updated by the CS5460A after an AC offset calibration sequence has been executed.

Referring to Figure 3, one should note that the AC offset registers affect the output results differently than the DC offset registers. The DC offset values are applied to the voltage/current signals very early in the signal path; the DC offset register value affects all CS5460A results. This is not true for the AC offset correction. The AC offset registers only affect the results of the rms-voltage/rms-current calculations.

Referring to Figure 3, the reader should note that there are separate calibration registers for the AC and DC offset corrections (for each channel). This is not true for gain corrections, as there is only one gain register per channel--AC and DC gain calibration results are stored in the same register. The results in the gain registers reflect either the AC or DC gain calibration results, whichever was performed most recently. Therefore, both a DC and AC offset can be applied to a channel at the same time, but only one gain calibration can be applied to each channel. Either AC or DC gain calibration can be used, but not both.

For both the voltage channel and the current channel, while the AC offset calibration sequence performs an entirely different function than the DC offset calibration sequence, the AC gain and DC gain calibration sequences perform the same function (but they accomplish the function using different techniques).

Since both the voltage and current channels have separate offset and gain registers associated with them, system offset or system gain can be performed on either channel without the calibration results from one channel affecting the other.

3.8.3 Calibration Sequence

1. The CS5460A must be operating in its *active* state, and ready to accept valid commands via the SPI interface, before a calibration sequence can be executed. Clearing the 'DRDY' bit in the Status Register is also recommended.

2. Apply appropriate calibration signal(s) to the "+" and "-" signals of the voltage/current channel input pairs. (The appropriate calibration signals for each type of calibration sequence are discussed next, in Sections 3.8.4 and 3.8.5.). The recommended sequence of calibration, if both gain and offset calibration are required, is to run offset calibration before gain calibration; and if both AC and DC offset calibration are required, DC offset should be calibrated first.

3. Next send the 8-bit calibration command to the CS5460A serial interface.

4. After the CS5460A has finished running the desired internal calibration sequence and has stored the updated calibration results in the appropriate calibration registers, the DRDY bit is set in the Status Register to indicate that the calibration sequence has been completed. If desired, the results of the calibration can now be read from the appropriate gain/offset registers, via the serial port.

Note that when the calibration command is sent to the CS5460A, the device must *not* be performing A/D conversions (in either of the two acquisitions modes). If the CS5460A is running A/D conversions/computations in the 'continuous computation cycles' acquisition mode (C = 1), the Power-Up/Halt Command must be issued first to terminate A/D conversions/computations. If the CS5460A is running A/D conversions/computations in the 'single computation cycle' data acquisition mode (C = 0), the Power-Up/Halt Command must be issued first (unless the computation cycle has completed) before executing any calibration sequence. The calibration sequences will not run if the CS5460A is running in either of the two available acquisition modes.

3.8.4 Calibration Signal Input Level

For both the voltage and current channels, the differential voltage levels of the calibration signals must be within the specified voltage input limits (refer to "Differential Input Voltage Range" in *Section 1., Characteristics & Specifications*). For the voltage channel the peak differential voltage level can never be more than 500 mV_{P-P}. The same is true for the current channel if the current channel input PGA is set for 10x gain. If the the current channel's PGA gain is set to 50x, then the current channel's input limits are 100 mV_{P-P}.

Note that for the AC/DC gain calibrations, there is an absolute limit on the RMS/DC voltage levels (respectively) that are selected for the voltage/current channel gain calibration input signals. The maximum value that the gain register can attain is 4. Therefore, for either channel, if the voltage level of a gain calibration input signal is low enough that it causes the CS5460A to attempt to set either gain register higher than 4, the gain calibration result will be invalid, and after this occurs, all CS5460A results obtained when the part is running A/D conversions will be invalid.

3.8.5 Calibration Signal Frequency

The frequency of the calibration signals must be less than 1 kHz (assume MCLK/K = 4.096 MHz and K = 1). Optimally, the frequency of the calibration signal will be at the same frequency as the fundamental power line frequency of the power system that is to be metered.

3.8.6 Input Configurations for Calibrations

Figure 16 shows the basic setup for gain calibration. If a DC gain calibration is desired, a *positive* DC voltage level must be applied, such that it truly represents the *absolute maximum* peak instantaneous voltage level that needs to be measured across the inputs (including the maximum over-range level that must be accurately measured). In other words, the input signal must be a positive DC voltage level that represents the desired absolute peak full-scale value. However, in many practical power metering situations, an AC signal is preferred over a DC signal to calibrate the gain. To perform AC gain calibration instead of DC, an AC reference signal should be applied that is set to the desired maximum RMS level. Because the voltage/current waveforms that must be measured in most power systems are approximately sinusoidal in nature, the RMS levels of the AC gain calibration input signals may need to be set significantly lower than the voltage/current channel's maximum DC voltage input level. This must be done in order to avoid the possibility that the peak values of the AC waveforms that are to be measured will not register a value that would be outside the available output code range of the voltage/current A/D converters. For example, on the voltage channel, if the Voltage Channel Gain Register is set to it's default power-on value of 1.000... before calibration, then the largest pure sinusoidal waveform that can be used in AC calibration is one whose RMS-value is ~0.7071 of the value of the voltage channel's peak DC input voltage value of 500 mV_{P-P}. Thus the maximum value of the input sinusoid would be ~176.78 mV (rms). But in many practical power metering situations, the RMS voltage input level of the AC gain calibration signal may be reduced even further, to allow for some over-ranging capability. A typical sinusoidal calibration value which allows for reasonable over-range margin would be 0.6 of the voltage/current channel's maximum input voltage level. For the voltage channel, such a sine-wave would have a value of 0.6 x 250 mV_{rms} = 150 mV_{rms}.

For the offset calibrations, there is no difference between the AC and DC calibration signals that must be supplied: simply connect the "+" and "-'

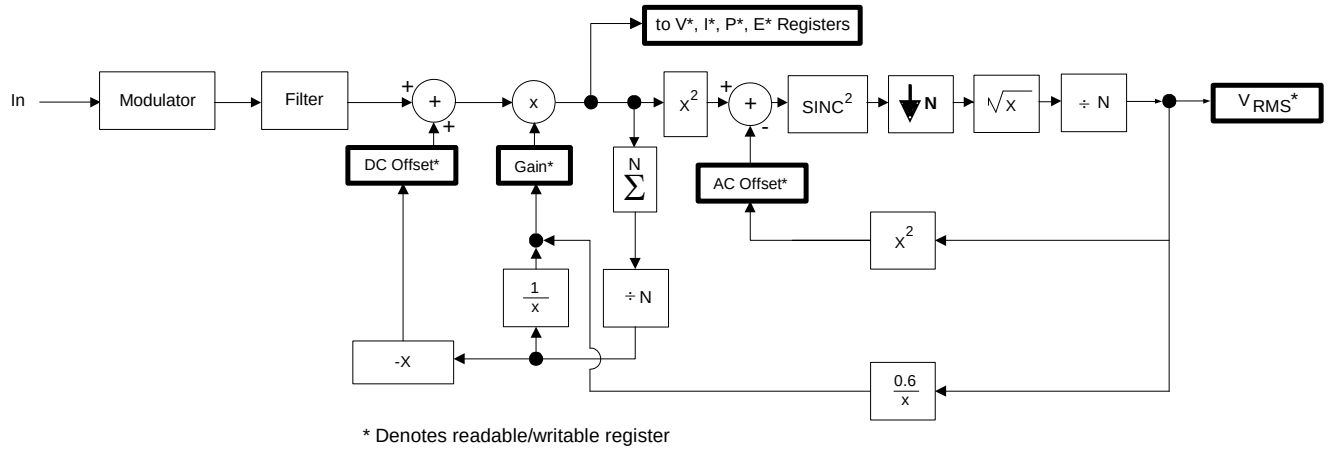


Figure 18. Calibration Data Flow

pins of the voltage/current channels to their ground reference level. (See Figure 17.)

Offset and gain calibration cannot be done at the same time. This will cause undesirable calibration results.

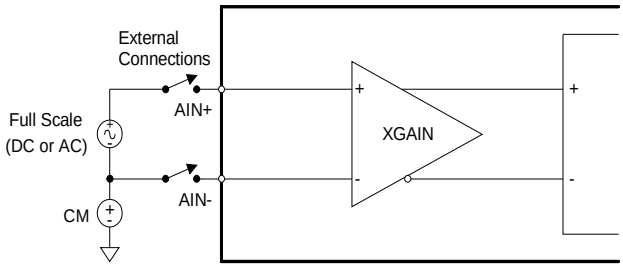


Figure 16. System Calibration of Gain.

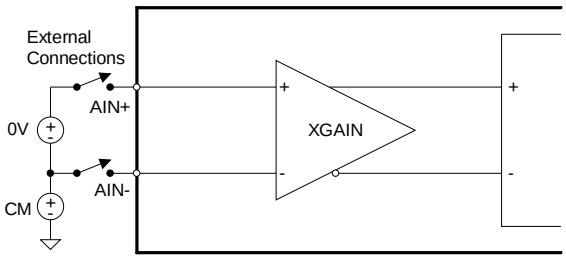


Figure 17. System Calibration of Offset.

3.8.7 Description of Calibration Algorithms

The computational flow of the CS5460A's AC and DC gain/offset calibration sequences are illustrated in Figure 18. This figure applies to both the voltage channel and the current channel. The following descriptions of calibration sequences will focus on the voltage channel, but apply equally to the current channel.

Note: For proper calibration, it is assumed that the value of the Voltage-/Current-Channel Gain Registers are set to default (1.0) before running the *gain* calibration(s), and the value in the Voltage-/Current Channel AC and DC *Offset* Registers is set to default (0) before running calibrations. This can be accomplished by a software or hardware reset of the device. The values in the voltage/current calibration registers *do* affect the results of the calibration sequences.

3.8.7.1 AC Offset Calibration Sequence

The idea of the AC offset calibration is to obtain an offset value that reflects the square of the RMS output level when the inputs are grounded. During normal operation, when the CS5460A is calculating the latest result for the RMS Voltage Register, this AC offset register value will be subtracted from the square of each successive voltage sample in order to nullify the AC offset that may be inherent in the voltage-channel signal path. Note that the value in the AC offset register is proportional to the *square* of the AC offset.

First, the inputs are grounded, and then the AC offset calibration command is sent to the CS5460A. When the AC offset calibration sequence is initiated, a valid RMS Voltage Register value is acquired and squared. This value is then subtracted from the square of each voltage sample that comes through the RMS data path. See Figure 18.

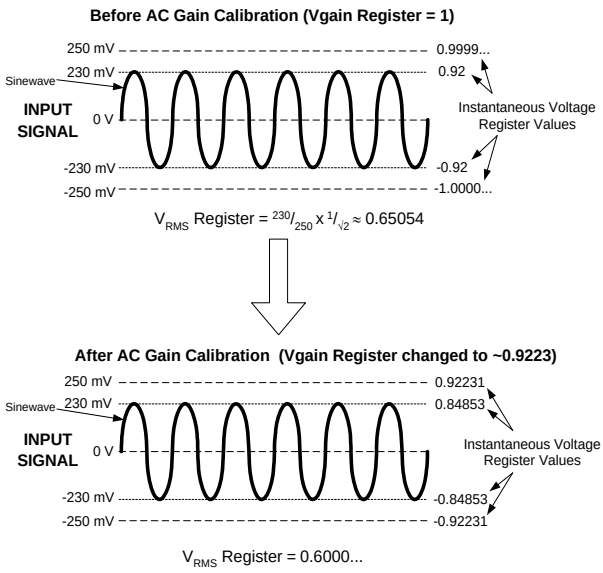


Figure 19. Example of AC Gain Calibration

3.8.7.2 DC Offset Calibration Sequence

The Voltage Channel DC Offset Register holds the negative of the simple average of N samples taken while the DC voltage offset calibration was executed. The inputs should be grounded during DC offset calibration. The DC offset value is added to the signal path to nullify the DC offset in the system.

3.8.7.3 AC Gain Calibration Sequence

The AC voltage gain calibration algorithm attempts to adjust the Voltage Channel Gain Register value such that the calibration reference signal level presented at the voltage inputs will result in a value of 0.6 in the RMS Voltage Register. The AC calibration signal is applied to the "+" and "-" input pins of the channel under calibration. During AC voltage gain calibration, the value in the RMS Voltage Register is divided into 0.6. This result is the AC gain calibration value stored in the Voltage Channel Gain Register.

3.8.7.4 DC Gain Calibration Sequence

Based on the level of the positive DC calibration voltage that should be applied across the "+" and "-" inputs, the CS5460A determines the Voltage Channel Gain Register value by averaging the Instantaneous Voltage Register's output signal values over one computation cycle (N samples) and then dividing this average into 1. Therefore, after the DC voltage gain calibration has been executed, the Instantaneous Voltage Register will read full-scale whenever the DC level of the input signal is equal to the level of the DC calibration signal that was applied to the voltage channel inputs during the DC gain calibration. For example, if a +230 mV DC signal is applied to the voltage channel inputs during the DC gain calibration for the current channel, then the Instantaneous Voltage Register will measure unity whenever a 230 mV DC level is applied to the voltage channel inputs.

3.8.8 Duration of Calibration Sequence

The value of the Cycle Count Register (N) determines the number of conversions that will be performed by the CS5460A during a given calibration sequence. For DC offset/gain calibrations, the calibration sequence always takes at least N + 30 conversion cycles to complete. For AC offset/gain calibrations, the calibration sequence takes at least 6N + 30 A/D conversion cycles to complete, (about 6 computation cycles). If N is increased, the accuracy of calibration results will increase.

For more information on Calibration, see *AN227*, "CALIBRATING THE CS5460A".

3.9 Phase Compensation

The values of bits 23 to 17 in the Configuration Register can be altered to adjust the amount of time delay that is imposed on the digitally sampled voltage channel signal. This time delay is applied to the voltage channel signal in order to compensate for the relative phase delay (with respect to the fundamental frequency) between the sensed voltage and current signals. Voltage and current transformers, as well as other sensor/filter/protection devices deployed at the front-end of the voltage/current sensor networks can often introduce a phase-delay in the system that distorts/corrupts the phase relationship between the line-voltage and line-current signals that are to be measured. The phase compensation bits PC[6:0] in the Configuration Register can be set to nullify this undesirable phase distortion between the digitally sampled signals in the two channels. The value in the 7-bit phase compensation word indicates the amount of time delay that is imposed on the volt-

age channel's analog input signal *with respect to* the current channel's analog input signal.

With the default setting, the phase delay on the voltage channel signal is ~0.995 µs (~0.0215 degrees assuming a 60 Hz power signal). With MCLK = 4.096 MHz and K = 1, the range of the internal phase compensation ranges from -2.8 degrees to +2.8 degrees when the input voltage/current signals are at 60 Hz. In this condition, each step of the phase compensation register (value of one LSB) is ~0.04 degrees. For values of MCLK other than 4.096 MHz, these values for the span (-2.8 to +2.8 degrees) and for the step size (0.04 degrees) should be scaled by 4.096 MHz / (MCLK / K). For power line frequencies other than 60Hz (e.g., 50 Hz), the values of the range and step size of the PC[6:0] bits can be determined by converting the above values to time-domain (seconds), and then computing the new range and step size (in degrees) with respect to the new line frequency.

Unlike offset/gain calibration, the CS5460A does not provide an automated on-chip phase calibration sequence. To calibrate the phase delay, the phase compensation bits can be adjusted while the CS5460A is running in 'continuous computation cycles' data acquisition mode. For example, the CS5460A can be set up to perform continuous computations on a *purely resistive load* (no inductance or capacitance). The PC[6:0] bits can then be adjusted until the Energy Register value is maximized.

3.10 Time-Base Calibration Register

The Time-Base Calibration Register (notated as "TBC" in Figure 3) is used to compensate for slight errors in the XIN input frequency. External oscillators and crystals have certain tolerances. If there is a concern about improving the accuracy of the clock for energy measurements, the Time-Base Calibration Register value can be manipulated to compensate for the frequency error. Note from Figure 3 that the TBC Register only affects the value in the Energy Register.

As an example, if the desired XIN frequency is 4.096 MHz, but during production-level testing, suppose that the average frequency of the crystal on a particular board is measured to actually be 4.091 MHz. The ratio of the desired frequency to the actual frequency is 4.096 MHz/4.091 MHz = ~1.00122219506. The TBC Register can be set to 1.00122213364 = 0x80280C(h), which is very close to the desired ratio.

3.11 Power Offset Register

Referring to Figure 3, note the "P_{off}" Register that appears just after the power computation. This register can be used to offset system power sources that may be resident in the system, but do not originate from the power line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power/energy measurement results. For example, even after DC offset and AC offset calibrations have been run on each channel, when a voltage signal is applied to the voltage channel inputs and the current channel is grounded (i.e., there is zero input on the current channel), the current channel may still register a very small amount of RMS current caused by leakage of the voltage channel input signal into the current channel input signal path. Although the CS5460A has high channel-to-channel crosstalk rejection, such crosstalk may not totally be eliminated.) If the amount of 'artificial' power that might be induced into the voltage/current channel signals due to such crosstalk/system noise/etc. can be determined, then the Power Offset Register can be programmed to nullify the effects of this unwanted energy.

3.12 Input Protection - Current Limit

In Figures 6, 7, 8, and 9, note the series resistor R_{I+} which is connected to the IIN+ input pin. This resistor serves two purposes. First, this resistor functions in coordination with C_{Idiff} and/or C_{Idiff} to form a low-pass filter. The filter will a) remove any broadband noise that is far outside of the frequency range of interest, and also b) this filter serves as the *anti-aliasing filter*, which is necessary to prevent the A/D converter from receiving input signals whose frequency is higher than one-half of the sampling frequency (the Nyquist frequency). The second purpose of this resistor is to provide current-limit protection for the Iin+ input pin, in the event of a power surge or lightning surge. The role that R_{I+} contributes to input filtering will be discussed in the Section 3.13. But first the current-limit protection requirements for the Iin+/Iin- and Vin+/Vin- pins are discussed.

The voltage/current-channel inputs have surge-current limits of 100 mA. This applies to brief voltage/current spikes (<250 ms). The limit is 10 mA for DC input overload situations. To prevent permanent damage to the CS5460A, the designer must include adequate protection circuitry in the power meter design, to insure that these pin current limits are never exceeded, when CS5460A is operating in the intended power-line metering environment.

Focusing specifically on Figure 7, which shows how voltage/current transformers can be used to sense the line-voltage/line-current, suppose for example that the requirements for a certain 120 VAC power system require that the power meter must be able to withstand up to a 8 kV voltage spike on the power line during normal operating conditions. To provide a suitable sensor voltage input level to the voltage channel input pins of the CS5460A, the turns ratio of the voltage-sense transformer should be chosen such that the ratio is, for example, on the order of 1000:1. A voltage-sense transformer with a 1000:1 turns ratio will provide a 120 mV (rms) signal to the CS5460A's differential voltage channel inputs, when the power line voltage is at the nominal level of 120 VAC. Therefore, a brief 8 kV surge would be reduced to a 8 V surge across R_{V+}.

What happens when 8 volts (common-mode) is present across one of the analog input pins of the CS5460A? The Vin+/Vin- and Iin+/Iin- pins of the CS5460A are equipped with internal protection diodes. If a voltage is presented to any of these pins that is larger than approximately 7 V (with respect to VA- pin) these protection diodes will turn on inside the CS5460A. But in order to prevent excessive current levels from flowing through the device, the value of R_{V+} must be large enough that when a 8V surge is present across the secondaries of the voltage-sense transformer, the brief surge current through R_{V+} should not be any greater than 100 mA. Therefore, a minimum value for R_{V+} would be (8 V - 7 V) / 100 mA = 10 Ω. This value may be increased as needed, to easily obtain the desired cutoff frequency of the anti-aliasing filter on the voltage channel (described later), and also to provide some margin. But the designer should try to avoid using values for the protection resistors that are excessively high. A typical value for R_{V+} would be 470 Ω.

The VIN- pin should also have a protection resistor (called R_{V-} in Figure 7). To maintain symmetry, the value of R_{V-} should be made equal to R_{V+}.

For the current channel inputs (Iin+ and Iin-), if the maximum current rating (I_{max}) for this power line is 30 A (RMS), then a suitable turns ratio for the current-sense transformer might be 200:1. Since the maximum load for a 120 VAC line rated at 30 A would be 4 Ω (for unity power factor), a brief 8 kV surge across "L" and "N" could generate as much as 2000 A (RMS) of current through the primaries of the current-sense transformer. This can in turn generate as much as 10 V across the secondaries of the current-sense transformer. This voltage is high enough to turn on one or more of the internal protection diodes located off of the Iin+/Iin- pins. Therefore, the value of the protection resistor that will limit the current flow to less than 100 mA would be (10 V - 7 V) / 100 mA = 30 Ω. In order to provide some margin and to use the same resistor values that are used on the Vin+/Vin- pins, a 470 Ω resistor can be used as a lower limit for the R_{I+} and R_{I-} resistors shown in Figure 7.

Referring to the circuit implementations shown in Figures 6, 8, and 9, note that when resistor-divider configurations are used to provide the voltage channel sense voltage, the VIN+ pin does not need an additional, separate, dedicated protection resistor. This is because the resistive voltage-divider already provides the series resistance that is needed for this protection resistance (from R_1 and R_2). (And note in Figure 8 that this is true for both the VIN+ pin and the VIN- pin.) In Figure 7, a voltage transformer is used as the voltage sensor. When any type of transformer is used as the sensor device for voltage (or current) channel, a dedicated protection resistor R_{V+} should be installed in series with the VIN+ pin, and similarly, a resistor (R_{V-}) should be installed in series to the VIN- input pin.

Additional considerations/techniques regarding the protection of the analog input pins against sudden high-frequency, high-level voltage/current surges are discussed in Section 3.14.

3.13 Input Filtering

Figure 6 shows how the analog inputs can be connected for a *single-ended* input configuration. Note here that the Vin- and Iin- input pins are held at a constant DC common-mode level, and the variation of the differential input signal occurs only on the Vin+ and Vin- pins. The common-mode level on the Vin-/Iin- pins is often set at (or very near) the CS5460A's common-mode ground reference potential. (The common-mode ground reference potential is defined by the voltage at the VA- pin.) But this is not required--the DC reference level of the Vin-/Iin- pins can be set to any potential between [VA-] and [(VA+) - 250 mV]. In Figure 6, observe the circuitry which has been placed in front of the current channel input pins, as one example. The anti-aliasing filter can be constructed by calculating appropriate values for $R_{I+} = R_{I-}$, C_{Idiff}, and $C_{I+} = C_{I-}$. The sensor voltage that is created by the voltage drop across R_{SHUNT} is fed into the Iin+ pin, while the voltage at the Iin- pin is held constant.

Figure 7 shows a *differential bipolar* input configuration. Note in Figure 7 that the "+" and "-" input pins for the voltage/current channels are equally referenced above and below the CS5460A's ground reference voltage. Such a differential bipolar input configuration can be used because the CS5460A voltage/current channel inputs are able to accept input voltage levels as low as -250 mV (common-mode) below the VA- pin ground reference, which is defined by the voltage at the VA- pin. (In fact, if desired, the center-tapped reference of these differential input pairs could be connected to a DC voltage of, for example, +2 V, because +2 V is within the available common-mode range of [VA-] and [VA+ - 250mV]. But this configuration may not be practical for most metering applications.) In the differential bipolar input configuration, the voltage signals at the Vin- and Iin- pins will fluctuate in similar fashion to the Vin+/Iin+ pins, except the voltages at the "-" pins will be 180 degrees out of phase with respect to the voltage signals at the "+" pins. Therefore the signal paths to the "+" and "-" pins play an equal role in defining the differential voltage input signal. Because of this, the protection resistors placed on Vin-/Iin- pins will play an equally important role as the resistors on the Vin+/Iin+ pins, in defining the differential responses of the voltage/current channel input anti-aliasing filters. These resistors also serve as the current-limit protection resistors (mentioned earlier).

Before determining a typical set of values for R_{V+}, R_{V-}, C_{V+}, C_{V-}, C_{Vdiff}, R_{I+}, R_{I-}, C_{I+}, C_{I-}, and C_{Idiff} in Figure 7, several other factors should be considered:

1. Values for the above resistors/capacitors should be chosen with the desired differential-mode (and common-mode) lowpass cutoff frequencies in mind. In general, the differential cutoff frequencies should not be less than 10 times the cut-off frequencies of the internal voltage/current channel filters, which can be estimated by studying Figure 4 and Figure 5. In these figures, the internal voltage channel cutoff frequency is ~1400 Hz while the current channel cutoff frequency is ~1600 Hz. If the cutoff frequency of the external anti-aliasing filter is much less than 10x these values (14000 Hz and 16000 Hz), then some of the harmonic content that may be present in the voltage/current signals will be attenuated by the voltage/current channel input anti-aliasing filters, because such R-C filters will begin to roll off at a frequency of 1/10th of the filter's -3 dB cutoff frequency. If the designer is not interested in metering energy that may be present in the higher harmonics (with respect to the fundamental power line frequency) then the differential-mode cutoff frequencies on the voltage/current input networks can be reduced. However, relaxing the metering bandwidth is usually unacceptable, as most modern power meters are required to register energy out to the 11th harmonic (at a minimum).

2. The first-order time-constants of the overall voltage and current channel sensor networks should be set such that they are equal (within reason), or at least close in magnitude. If the time-constants of the voltage/current sensor networks are not well-matched, then the phase relationship between the voltage-sense and current-sense signals will suffer an undesirable shift. In this situation, the real (true) power/energy measurements reported by the CS5460A can contain significant error, because the power factor of the sensed voltage and current signals will be significantly different than the actual power factor of the power line voltage/current waveforms.

Note also that in addition to the time-constants of the input R-C filters, the phase-shifting properties of the voltage/current sensors devices may also contribute to the overall time-constants of the voltage/current input sensor networks. For example, current-sense transformers and potential transformers can impose phase-shifts on the sensed current/voltage waveforms. Therefore, this possible source of additional phase-shift caused by sensor devices may also need to be considered while selecting the final R and C values for the voltage/current anti-aliasing filters. As an alternative to, or in addition to the fine adjustment of the R and C values of the two anti-alias filters, the CS5460A's phase compensation bits (see *Phase Compensation*) can also be adjusted, in order to more closely match the overall time-constants of the voltage/current input networks. Regardless of whether the phase compensation bits are or are not used to help more closely match the time-constants, this requirement of equal time-constants must ultimately be considered when selecting the final R and C values that will be used for the input filters. (Of course, this factor may not turn out to be so important if the designer is confident that the mis-match between the voltage/current channel time-constants will not cause enough error to violate the accuracy requirements for the given power/energy metering application.)

3. Referring to the specs in *Section 1*, note that the differential input impedance across the current channel input pins is only 30 kΩ, which is significantly less than the corresponding impedance across the voltage channel input pins (which is 1 MΩ). While the impedance across the voltage channel is usually high enough to be ignored, the impedance across the current channel inputs may need to be taken into account by the designer when the desired cutoff frequencies of the filters (and the time-constants of the overall input networks) are computed. Also, because of this rather low input impedance across the current channel inputs, the designer should note that as the values for R_{I+} and/or R_{I-} are increased, the interaction of the current channel's input impedance can begin to cause a significant voltage drop within the current channel input network. If this is not taken into account, values may be chosen for $R_{I+} = R_{I-}$ that are large enough to cause a discrepancy between the expected (theoretical) sensor gain and the *actual* sensor gain of the current sensor network, which may not be anticipated by the designer. Also, if this voltage drop effect is not considered, the designer may select values for R_{I+} and R_{I} that are slightly larger than they should be, in terms of maximizing the available dynamic range of the current channel input. For the very same reason, the line-current-to-sensor-output-voltage conversion factor of the current sensor may not be optimized if this voltage division is not considered, when (for example) selecting a value for the burden resistor for a given current transformer. This issue should be considered, although a slight voltage drop only causes a slight loss in available dynamic range, and the effects of this voltage drop on the actual current channel sensor gain can be removed during gain calibration of the current channel.

4. Referring to Figures 6 - 9, not all of the capacitors/resistors shown in these example circuit diagrams are necessary; however, note that the all of the filter capacitors (C_{V+}, C_{V-}, C_{I+}, C_{I-}, C_{Vdiff}, and C_{Idiff}) can, in some situations, help to improve the ability of both input networks to attenuate very high-frequency RFI that can enter into the CS5460A's analog input pins. Therefore, during layout of the PCB, these capacitors should be placed in close proximity to their respective input pins.

If any/all of the common-mode connected capacitors (C_{V+}, C_{V-}, C_{I+}, C_{I-}) are included in the input networks, their values should be selected such that they are at least one order of magnitude *smaller* than the value of the differential capacitors (C_{Vdiff}, and C_{Idiff}). This is done for at least two reasons:

a) The value tolerance for most types of commercially available surface-mount capacitors is not small enough to insure appreciable value matching, between the value of C_{V+} vs. C_{V-}, as well as between the value of C_{V+} vs. C_{V-}. Such value mismatch can adversely affect the desired differential-mode response of the voltage/current input networks. By keeping the values of these common-mode capacitors small, and allowing the value of the C_{Vdiff}, and C_{Idiff} to dominate the *differential* 1st-order time-constant of the input filter networks, this undesirable possibility of frequency response variation can be minimized.

b) The common-mode rejection performance of the CS5460A is sufficient within the frequency range over which the CS5460A performs A/D conversions. Addition of such common-mode caps can actually often degrade the common-mode rejection performance of the entire voltage/current input networks. Therefore, choosing relatively small values for (C_{V+}, C_{V-}, C_{I+}, C_{I-}) will provide necessary common-mode rejection at the much higher frequencies, and will allow the CS5460A to realize its CMRR performance in the frequency-range of interest.

[Note that this discussion does not include correction of phase-shifts caused by the voltage-sense transformer and current-sense transformer, although these phase-shifts should definitely be considered in a real-life practical meter design.] On the current channel, using commonly available values for the components, R_{I+} and R_{I-} can be set to 470 Ω. Then a value of C_{Idiff} = 18 nF and a value of 0.22 nF for C_{I-} and C_{I-} will yield a -3 dB cutoff frequency of 15341 Hz for the current channel. For the voltage channel, if R_{I+} and R_{I-} are also set to 470 Ω, C_{Vdiff} = 18 nF, and C_{V-} = C_{V-} = 0.22 nF (same as current channel), the -3 dB cutoff frequency of the voltage channel's input filter will be 14870 Hz. The difference in the two cutoff frequencies is due to the difference in the input impedance between the voltage/current channels.

If there is concern about the effect that the difference in these two cutoff frequencies (and therefore the mis-match between the time-constants of the overall voltage/current input networks) would have on the accuracy of the power/energy registration, a non-standard resistor value for R_{V+} = R_{V-} of (for example) 455 Ω can be used. This would shift the (differential) -3 dB cutoff frequency of the voltage channel's input filter (at the voltage channel inputs) to ~15370 Hz, which would cause the first-order time-constants of the voltage/current channel input filters to be closer in value.

Agreement between the voltage/current channel time-constants can also be obtained by adjusting the phase compensation bits, instead of using less commonly-available resistor/capacitor values (such as R_{I+} = R_{I-} = 455 Ω). If the values of R_{I+} and R_{I-} are again 470 Ω, the first-order time-constants of the two R-C filters are estimated by taking the reciprocal of the -3 dB cutoff frequencies (when expressed in rads/s). Subtracting these two time-constants shows that after the voltage/current signals pass through their respective anti-aliasing filters, the sensed voltage signal will be delayed ~0.329 µs more than the current signal. If metering a 60 Hz power system, this implies that the input voltage-sense signal will be delayed ~0.007 degrees more than the delay imposed on the input current-sense signal. Note that when the PC[6:0] bits are set to their default setting of "0000000", the internal filtering stages of the CS5460A will impose an additional delay on the fundamental frequency component of the 60Hz voltage signal of 0.0215 degrees, with respect to the current signal. The total difference between the delay on the voltage-sense fundamental and the current-sense fundamental will therefore be ~0.286 degrees. But if the phase compensation bits are set to 1111111, the CS5460A will delay the voltage channel signal by an additional -0.04 degrees, which is equivalent to shifting the voltage signal *forward* by 0.04 degrees. The total phase shift on the voltage-sense signal (with respect to the fundamental frequency) would then be ~0.011 degrees ahead of the current-sense signal, which would therefore provide more closely-matched delay values between the voltage-sense and current-sense signals. Adjustment of the PC[6:0] bits therefore can provide an effective way to more closely match the delays of the voltage/current sensor signals, allowing for more commonly available R and C component values to be used in both of these filters.

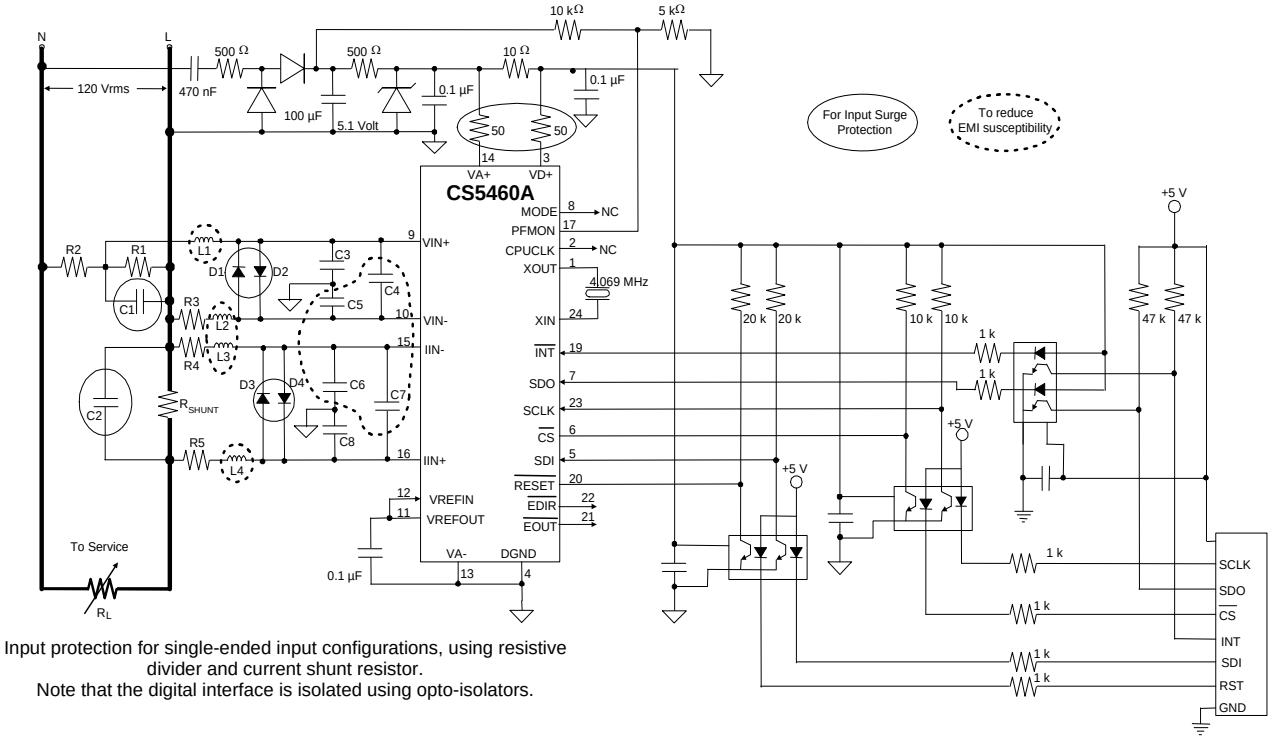
As a final note, tolerances of the R and C components that are used to build the two R-C filters should also be taken into consideration. A common tolerance of ±0.1% can vary the delay by as much as much as ~±2.07 µs, which means that the *difference* between the delays of the voltage-sense and current-sense signals that is caused by these filters could vary by as much as ~±4.1 µs, which is equivalent to a phase shift of ~±0.089 degrees (at 60 Hz). This in turn implies that our decision to adjust the PC[6:0] bits (to shift the voltage signal forward by 0.04 degrees) could actually cause the voltage signal to be shifted by as much as ~0.100 degrees ahead of the current signal. Thus, adjustment of the PC[6:0] bits to more closely match the two time-constants/delays may only be useful if a precise calibration operation can be

performed on *each* individual power meter, during final calibration/test of the meter.

3.14 Protection Against High-voltage and/or High-current Surges

In many power distribution systems, it is very likely that the power lines will occasionally carry brief but large transient spikes of voltage/current. Two common sources of such high-energy disturbances are 1) a surge in the line during a lightning storm, or 2) a surge that is caused when a very inductive or capacitive load on the power line is suddenly turned on ("inductive kick"). In these situations, the input protection resistors and corresponding input filter capacitors (discussed in the previous sections) may not be sufficient to protect the CS5460A from such high-frequency voltage/current surges. The surges may still be strong enough to cause permanent damage to the CS5460A. Because of this, the designer should consider adding certain additional components within the voltage/current channel input circuitry, which can help to protect the CS5460A from being permanently damaged by the surges.

Referring to Figure 20, the addition of capacitors C1 and C2 can help to further attenuate these high-frequency power surges, which can greatly decrease the chances that the CS5460A will be damaged. Typical values for C1 and C2 may be on the order of 10 pF, although the exact value is related to the reactive and resistive properties of the voltage and current sensor devices. In addition, diodes D1 - D4 can help to quickly clamp a high voltage surge voltage presented across the voltage/current inputs, before such a surge can damage the CS5460A. An example of a suitable diode part number for this application is BAV199, which has the ability to turn on very quickly (very small turn-on time). A fuse could potentially serve this purpose as well (not shown). R3 and R4 can provide protection on the "-" sides of the two input pairs. Set R3 = R1 and R4 = R5. Finally, placing 50 Ω resistors in series with the VA+ and VD+ pins is another technique that has sometimes proven to be effective in protecting the CS5460A from such high-level, high-frequency voltage/current surges. However, these 50 Ω resistors may not be necessary if the protection on the analog input channels is sufficient, and this is not the most attractive so-



Input protection for single-ended input configurations, using resistive divider and current shunt resistor.
Note that the digital interface is isolated using opto-isolators.

Figure 20. Input Protection for Single-Ended Input Configurations

lution, because these resistors will dissipate what can be a significant amount of power, and they will cause an undesirable voltage drop which decreases the voltage level presented to the VA+ and VD+ supply pins.

3.15 Improving RFI Immunity

During EMC acceptance testing of a power metering assembly, the performance of the CS5460A's A/D converters can be adversely affected by external radio frequency interference (RFI). Such external RFI can be coupled into the copper traces and/or wires on the PCB. If RFI is coupled into any of the traces which tie into the CS5460A's Vin+/Vin- or Iin+/Iin- input pins, then errors may be present in the CS5460A's power/energy registration results.

When such degradation in performance is detected, the CS5460A's immunity to RF disturbance may be improved by configuring the '+' and '-' inputs of the voltage/current channel inputs such that they are more symmetrical. This is illustrated in Figure 20 with the addition of resistors R3 and R4, as well as capacitors C5 and C6. Note that the input circuitry placed in front of the voltage/current channel inputs in Figure 20 represents a *single-ended* input configurations (for both channels). Therefore, these extra resistors and components may not necessarily be needed to achieve the simple basic anti-aliasing filtering on the inputs. However, the addition of these extra components can create more symmetry across the '+' and '-' inputs of the voltage/current input channels, which can often help to reduce the CS5460A's susceptibility to RFI. The value of C5 should be the same as C3, (and so the designer may have to re-calculate the desired value of C3, since the addition of C5 will change the overall differential-/common-mode frequency responses of the input filter.) A similar argument can be made for the addition of C6 (to match C8) on the current channel's input filter. Finally, addition of capacitors C4 and C7 can also sometimes help to improve CS5460A's performance in the presence of RFI. All of these input capacitors (C3 - C8) should be placed in very close proximity to the '+' and '-' pins of the voltage/current input pins in order to maximize their ability to protect the input pins from high-frequency RFI. In addition to or as an alternative to these capacitors, addition of inductors L1 - L4 can sometimes help to suppress any incoming RFI. Note that the additional components just discussed can sometimes actually *degrade* the CS5460A's immunity to RFI. The exact configuration that works best can vary significantly, according to the exact PCB layout/orientation. Finally, note that inside the CS5460A, the Vin+, Vin-, Iin+, and Iin- pins have all been buffered with ~10 pF of internal capacitance (to VA-) in attempt to improve the device's immunity to external RFI.

3.16 PCB Layout

For optimal performance, the CS5460A should be placed entirely over an analog ground plane with both the VA- and DGND pins of the device connected to the analog plane.

Note: Refer to the CDB5460A Evaluation Board for suggested layout details, as well as Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

4. SERIAL PORT OVERVIEW

The CS5460A's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8 bit command words on the rising edge of SCLK. Upon decoding of the command word, the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers are used to control the ADC's functions. All registers are 24-bits in length. Figure 21, in section 5, summarizes the internal registers available.

The CS5460A is initialized and fully operational in its *active* state upon power-on. After a power-on, the device will wait to receive a valid command (the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word, the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register.

4.1 Commands (Write Only)

All command words are 1 byte in length. Commands that write to a register must be followed by 3 bytes of register data. Commands that read from registers initiate the output of 3 bytes of register data. Commands that read data can be 'chained' with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed). This allows for 'chaining' commands.

4.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

Modes of acquisition/measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

4.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. It can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

4.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. It can also serve as a NOP command.

4.1.4 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down into either *stand-by* or *sleep* power saving mode (See *4.1.5*), this command will power-up the device. After the CS5460A is initially powered-on, no conversions/computations will be running. If the device is already powered on and the device is running either 'single computation cycle' or 'continuous computation cycles' data acquisition modes, all computations will be halted once this command is received.

4.1.5 Power-Down

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down states to conserve power. If the chip is put in stand-by state, all circuitry except the analog/digital clock generators is turned off. In the sleep state, all circuitry except the digital clock generator and the instruction decoder is turned off. Waking up the CS5460A out of sleep state requires more time than waking the device out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog clock signal.

[S1 S]0 Power-down state
00 = Reserved
01 = Halt and enter stand-by power saving state. This state allows quick power-on time
10 = Halt and enter sleep power saving state. This state requires a slow power-on time
11 = Reserved

4.1.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	V	I	R	G	O

The device has the capability of performing a system AC offset calibration, DC offset calibration, AC gain calibration, and DC gain calibration. Calibration can be done on the voltage channel, the current channel, or both channels at the same time. Offset and gain calibrations should NOT be performed at the same time (must do one after the other). For a given application, if DC gain calibrations are performed, then AC gain calibration should not be performed (and vice-versa). The proper input voltages must be supplied to the device before initiating calibration.

[V I] Designates calibration channel
00 = Not allowed
01 = Calibrate the current channel
10 = Calibrate the voltage channel
11 = Calibrate voltage and current channel simultaneously

R Specifies AC calibration (R=1) or DC calibration (R=0)

G Designates gain calibration
0 = Normal operation
1 = Perform gain calibration

O Designates offset calibration
0 = Normal operation
1 = Perform offset calibration

4.1.7 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

This command informs the state machine that a register access is required. On reads the addressed register is loaded into the output buffer and clocked out by SCLK. On writes the data is clocked into the input buffer and transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits. Binary encoded 0 to 31. All registers are 24 bits in length.

Address	Abbreviation	Name/Description
00000	Config	Configuration Register.
00001	I_{DCoff}	Current Channel DC Offset Register.
00010	I_{gn}	Current Channel Gain Register.
00011	V_{DCoff}	Voltage Channel DC Offset Register.
00100	V_{gn}	Voltage Channel Gain Register.
00101	Cycle Count	Number of A/D cycles per computation cycle.
00110	Pulse-Rate	Used to set the energy-to-pulse ratio on $\overline{EOUT}$ (and $\overline{EDIR}$).
00111	I	Instantaneous Current Register (most recent current sample).
01000	V	Instantaneous Voltage Register (most recent voltage sample).
01001	P	Instantaneous Power Register (most recent power sample).
01010	E	Energy Register (accumulated over latest computation cycle).
01011	I_{RMS}	RMS Current Register (computed over latest computation cycle).
01100	V_{RMS}	RMS Voltage Register (computed over latest computation cycle).
01101	TBC	Timebase Calibration Register.
01110	Poff	Power Offset Register.
01111	Status	Status Register.
10000	I_{ACoff}	Current Channel AC Offset Register.
10001	V_{ACoff}	Voltage Channel AC Offset Register.
10010	Res	Reserved †
.	.	.
.	.	.
10111	Res	Reserved †
11000	Res	Reserved †
11001	Test	Reserved †
11010	Mask	Mask Register.
11011	Res	Reserved †
11100	Ctrl	Control Register.
11101	Res	Reserved †
.	.	.
.	.	.
11111	Res	Reserved †

† These registers are for Internal Use only and should not be written to.

4.2 Serial Port Interface

The CS5460A's *slave-mode* serial interface consists of two control lines and two data lines, which have the following pin-names: $\overline{CS}$, SCLK, SDI, SDO. Each control line is now described.

$\overline{CS}$ Chip Select (input pin), is the control line which enables access to the serial port. When $\overline{CS}$ is set to logic 1, the SDI, SDO, and SCLK pins will be held at high impedance. When the $\overline{CS}$ pin is set to logic 0, the SDI, SDO, and SCLK pins have the following functionality:

SDI Serial Data In (input pin), is the user-generated signal used to transfer (send) data/command/address/etc. bits into the device.

SDO Serial Data Out (output pin), is the data signal used to read output data bits from the device's registers.

SCLK Serial Clock (input pin), is the serial bit-clock which controls the transfer rate of data to/from the ADC's serial port. To accommodate opto-isolators, SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

4.3 Serial Read and Write

The state machine decodes the command word as it is received. Data is written to and read from the CS5460A by using the Register Read/Write command. Figure 1 illustrates the serial sequence necessary to write to or read from the serial port buffers. As shown in Figure 1, a transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). It is important to note that some commands use information from the Cycle-Count Register and Configuration Register to perform the function. For those commands, it is important that the correct information is written to those registers first.

4.3.1 Register Write

When a command involves a write operation, the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the next 24 SCLK cycles. Command words instructing a register write must be followed by 24 bits of data. For instance, to write the Configuration Register, the command (0x40) is transmitted to initiate a write to the Configuration Register. The CS5460A will acquire the serial data input from the SDI pin after 24 pulses on the SCLK pin. Once the data is received, the state machine writes the data to the Configuration Register and then waits to receive another valid command.

4.3.2 Register Read

When a read command is initiated, the serial port will start transferring register content bits (MSB first) on the SDO pin for the next 8, 16, or 24 SCLK cycles. Command words instructing a register read may be terminated at 8-bit boundaries (e.g., read transfers may be 8, 16, or 24 bits in length). Also, data register reads allow "command chaining", in which the micro-controller is allowed to send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the first register read. For example, if a command word is sent to the state machine to read one of the output registers, then after pulsing SCLK for 16-bits of data, a second write command word (e.g., to clear the Status Register) may be pulsed on to the SDI line at the same time the last 8-bits of data (from the first read command) are pulsed from the SDO line.

During the read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.

4.4 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by writing a logic 1 to the RS (Reset System) bit in the Configuration Register, which automatically returns to logic 0 after reset. At the end of the 32nd SCLK (i.e., 8 bit command word and 24 bit data word) internal synchronization delays the loading of the Configuration Register by 3 or 4 DCLK cycles. Then the reset circuit initiates the reset routine on the 1st falling edge of MCLK.

A hardware reset is initiated when the $\overline{RESET}$ pin is forced low for *at least* 50 ns. The $\overline{RESET}$ signal is asynchronous, requiring no MCLKs for the part to detect and store a reset event. The $\overline{RESET}$ pin is a Schmitt Trigger input, which allows it to accept

slow rise times and/or noisy control signals. (It is not uncommon to experience temporary periods of abnormally high noise and/or slow, gradual restoration of power, during/after a power "black-out" or power "brown-out" event.) Once the RESET pin is de-asserted, the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for 12 MCLK cycles after RESET is de-asserted. After a hardware or software reset, the internal registers (some of which may drive output pins) will be reset to their default values on the first MCLK received after detecting a reset event (see Table 3). The CS5460A will then assume its *active* state. (The term *active state*, as well as the other possible power states of the CS5460A, are described in Section 4.6).

The reader should refer to Section 5 for a complete description of the registers listed in Table 3.

Configuration Register:	0x000001
DC offset registers:	0x000000
Gain registers	0x400000
Pulse-Rate Register:	0x0FA000
Cycle-Counter Register:	0x000FA0
Timebase Register:	0x800000
Status Register:	(see Section 5)
Mask Register:	0x000000
Control Register:	0x000000
AC offset registers:	0x000000
Power Offset Register:	0x000000
All data registers:	0x000000
All unsigned data registers	0x000000

Table 3. Default Register Values upon Reset Event

4.5 Serial Port Initialization

It is possible for the serial interface to become unsynchronized with respect to the SCLK input. If this occurs, any attempt to clock valid CS5460A commands into the serial interface will result in either no operation or unexpected operation because the CS5460A will not interpret the input command bits correctly. The CS5460A's serial port must then be re-initialized. To initialize the serial port, any of the following actions can be performed:

1) Power on the CS5460A. (Or if the device is already powered on, recycle the power.)
2) Hardware Reset.
3) Issue the *Serial Port Initialization Sequence*, which is performed by clocking 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE) to the serial interface.

4.6 CS5460A Power States

Active state denotes the operation of CS5460A when the device is fully powered on (i.e., not in *sleep* state or *stand-by* state). Performing any of the following actions will insure that the CS5460A is operating in the *active* state:

1) Power on the CS5460A. (Or if the device is already powered on, recycle the power.)
2) Hardware Reset
3) Software Reset

In addition to the three actions listed above, if the device is operating in *sleep* state or *stand-by* state, waking up the device out of *sleep* state or *stand-by* state (by issuing the Power-Up/Halt command) will also insure that the device is set into *active* state. But in order to send the Power-Up/Halt command to the device, the serial port has to be initialized. Therefore, successful wake-up of the device can be insured by writing the serial port initialization sequence to the serial interface, prior to writing the Power-Up/Halt command.

For a description of the *sleep* power state and the *stand-by* power state, see the Power Down Command, located in Section 4.1.

5. REGISTER DESCRIPTIONS

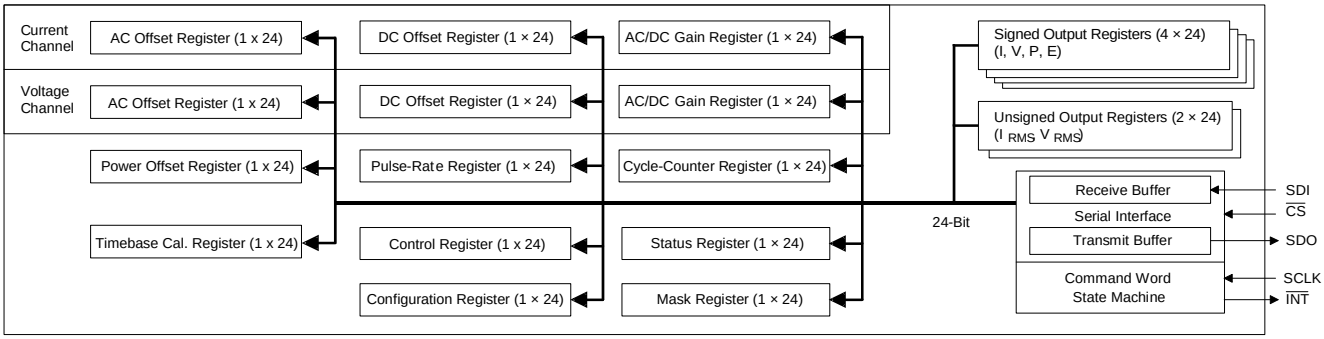


Figure 21. CS5460A Register Diagram

Note: 1. ** "default" => bit status after software or hardware reset

2. Note that all registers can be read from, and written to.

5.1 Configuration Register

Address: 0

23	22	21	20	19	18	17	16
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Gi
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA	Res	Res	SI1	SI0	EOD	DL1	DL0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RS	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

K[3:0] Clock divider. A 4 bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. Note that a value of "0000" will set K to 16 (not zero).

iCPU Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

IHPF Control the use of the High Pass Filter on the Current Channel.
0 = High-pass filter is disabled. If VHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter is enabled.

VHPF Control the use of the High Pass Filter on the voltage Channel.
0 = High-pass filter is disabled. If IHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter enabled

RS	Start a chip reset cycle when set 1. The reset cycle lasts for less than 10 XIN cycles. The bit is automatically returned to 0 by the reset cycle.
DL0	When EOD = 1, $\overline{\text{EDIR}}$ becomes a user defined pin. DL0 sets the value of the $\overline{\text{EDIR}}$ pin. Default = '0'
DL1	When EOD = 1, $\overline{\text{EOUT}}$ becomes a user defined pin. DL1 sets the value of the $\overline{\text{EOUT}}$ pin. Default = '0'
EOD	Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be controlled by the DL0 and DL1 bits. $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ can also be accessed using the Status Register. 0 = Normal operation of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins. (default) 1 = DL0 and DL1 bits control the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins.
SI[1:0]	Soft interrupt configuration. Select the desired pin behavior for indication of an interrupt. 00 = active low level (default) 01 = active high level 10 = falling edge (INT is normally high) 11 = rising edge (INT is normally low)
Res	Reserved. These bits must be set to zero.
EWA	Allows the output pins of $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ of multiple chips to be connected in a wire-AND, using an external pull-up device. 0 = normal outputs (default) 1 = only the pull-down device of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins are active
Gi	Sets the gain of the current PGA 0 = gain is 10 (default) 1 = gain is 50
PC[6:0]	Phase compensation. A 2's complement number used to set the delay in the voltage channel. When MCLK = 4.096 MHz and K = 1, the phase adjustment range is about -2.8 to +2.8 degrees and each step is about 0.04 degrees (this assumes that the power line frequency is 60 Hz). If (MCLK / K) is not 4.096 MHz, the values for the range and step size should be scaled by the factor 4.096 MHz / (MCLK / K). Default setting is 0000000 = 0.0215 degrees phase delay (when MCLK = 4.096 MHz).

5.2 Current Channel DC Offset Register and Voltage Channel DC Offset Register

Address: 1 (Current Channel DC Offset Register)
3 (Voltage Channel DC Offset Register)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

The DC offset registers are initialized to zero on reset, allowing the device to function and perform measurements. The register is loaded after one computation cycle with the current or voltage offset when the proper input is applied and the DC Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range ± full scale. The numeric format of this register is two's complement notation.

5.3 Current Channel Gain Register and Voltage Channel Gain Register

Address: 2 (Current Channel Gain Register)
4 (Voltage Channel Gain Register)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The gain registers are initialized to 1.0 on reset, allowing the device to function and perform measurements. The gain registers hold the result of either the AC or DC gain calibrations, whichever was most recently performed. If DC calibration is performed, the register is loaded after one computation cycle with the system gain when the proper DC input is applied and the Calibration Command is received. If AC calibration is performed, then after ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register) the register(s) is loaded with the system gain when the proper AC input is applied and the Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range $0.0 \leq \text{Gain} < 4.0$.

5.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default** = 4000

The Cycle Count Register value (denoted as 'N') specifies the number of A/D conversion cycles per *computation cycle*. For each computation cycle, the updated results in the RMS and Energy Registers are computed using the most recent set of N continuous instantaneous voltage/current samples. When the device is commanded to operate in 'continuous computation cycles' data acquisition mode, the computation cycle frequency is (MCLK / K) / (1024 ∗ N) where MCLK is master clock input frequency (into XIN / XOUT pins), K is the clock divider value (as specified in the Configuration Register), and N is Cycle Count Register value.

5.5 Pulse-Rate Register

Address: 6

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00Hz

The Pulse-Rate Register determines the frequency of the train of pulses output on the $\overline{EOUT}$ pin. Each $\overline{EOUT}$ pulse represents a predetermined magnitude of real (billable) energy. The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments.

5.6 I,V,P,E Signed Output Register Results

Address: 7 - 10

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

These signed registers contain the last value of the measured results of I, V, P, and E. The results are in the range of $-1.0 \le I, V, P, E < 1.0$. The value is represented in two's complement notation, with the binary point place to the right of the MSB (which is the sign bit). I, V, P, and E are output results registers which contain signed values. Note that the I, V, and P Registers are updated every conversion cycle, while the E Register is only updated after each computation cycle. The numeric format of this register is two's complement notation.

5.7 I_{RMS}, V_{RMS} Unsigned Output Register Results

Address: 11,12

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

These unsigned registers contain the last value of the calculated results of I_{RMS} and V_{RMS}. The results are in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$. The value is represented in binary notation, with the binary point place to the left of the MSB. I_{RMS} and V_{RMS} are output result registers which contain unsigned values.

5.8 Timebase Calibration Register

Address: 13

MSB															LSB
2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 1.000

The Timebase Calibration Register is initialized to 1.0 on reset, allowing the device to function and perform computations. The register can be loaded with the clock frequency error to compensate for a gain error caused by the crystal/oscillator tolerance. The value is in the range $0.0 \le TBC < 2.0$.

5.9 Power Offset Register

Address: 14

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

This offset value is added to each power value that is computed for each voltage/current sample pair before being accumulated in the Energy Register. The numeric format of this register is two's complement notation. This register can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system.

5.10 Current Channel AC Offset Register and Voltage Channel AC Offset Register

Address: 16 (Current Channel AC Offset Register)
17 (Voltage Channel AC Offset Register)

MSB															LSB
2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	.....	2^{-30}	2^{-31}	2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}

Default** = 0.000

The AC offset registers are initialized to zero on reset, allowing the device to function and perform measurements. First, the ground-level input should be applied to the inputs. Then the AC Offset Calibration Command is should be sent to the CS5460A. After ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register), the gain register(s) is loaded with the square of the system AC offset value. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. Note that this register value represents the square of the AC current/voltage offset.

5.11 Status Register and Mask Register

Address: *15* (Status Register)
26 (Mask Register)

23	22	21	20	19	18	17	16
DRDY	EOUT	EDIR	CRDY	MATH	Res	IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWOR	IROR	VROR	EOR	EOOR	Res	ID3	ID2
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ID1	ID0	WDT	VOD	IOD	LSD	0	$\overline{IC}$

Default** = Binary: 00000000000000xxxx000001 (Status Register) {x = state depends on device revision}

Binary: 000000000000000000000000 (Mask Register)

The Status Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can write logic '1' values back to the Status Register to selectively clear only those bits that have been resolved/registered by the system MCU, without concern of clearing any newly set bits. Even if a status bit is masked to prevent the interrupt, the corresponding status bit will still be set in the Status Register so the user can poll the status.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the Mask Register will

allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit becomes active.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 when the part is given an invalid command. Can be deactivated only by sending a port initialization sequence to the serial port (or by executing a software/hardware reset). When writing to the Status Register, this bit is ignored.

LSD — Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (PMLO), with respect to VA- pin. For a given part, PMLO can be as low as 2.3 V. LSD bit cannot be permanently reset until the voltage at PFMON pin rises back above the high-voltage threshold (PMHI), which is typically 100mV above the device's low-voltage threshold. PMHI will never be greater than 2.7 V.

IOD — Modulator oscillation detect on the current channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

VOD — Modulator oscillation detect on the voltage channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

Note: The IOD and VOD bits may be 'falsely' triggered by very brief voltage spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD and VOD bits will re-assert themselves even after being cleared, multiple times.

WDT — Watch-Dog Timer. Set when there has been no reading of the Energy Register for more than 5 seconds. (MCLK = 4.096 MHz, K = 1) To clear this bit, first read the Energy Register, then write to the Status Register with this bit set to logic '1'. When MCLK/K is not 4.096 MHz, the time duration is 5 * [4.096 MHz / (MCLK/K)] seconds.

ID3:0 — Revision/Version Identification.

EOOR — The internal $\overline{EOUT}$ Energy Accumulation Register went out of range. Note that the $\overline{EOUT}$ Energy Accumulation Register is different than the Energy Register available through the serial port. This register cannot be read by the user. Assertion of this bit can be caused by having an output rate that is too small for the power being measured. The problem can be corrected by specifying a higher frequency in the Pulse-Rate Register.

EOR — Energy Out of Range. Set when the Energy Register overflows, because the amount of energy that has been accumulated during the pending computation cycle is greater than the register's highest allowable positive value or below the register's lowest allowable negative value.

VROR — RMS Voltage Out of Range. Set when the calibrated RMS voltage value is too large to fit in the RMS Voltage Register.

IROR — RMS Current Out of Range. Set when the calibrated RMS current value is too large to fit in the RMS Current Register.

PWOR — Power Calculation Out of Range. Set when the *magnitude* of the calculated power is too large to fit in the Instantaneous Power Register.

VOR — Voltage Out of Range.

IOR — Current Out of Range. Set when the *magnitude* of the calibrated current value is too large or too small to fit in the Instantaneous Current Register.

MATH — General computation Indicates that a divide operation overflowed. This can happen normally in the course of computation. If this bit is asserted but no other bits are asserted, then there is no error, and this bit should be ignored.

CRDY — Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate, which is usually 4 kHz.

EDIR — Set whenever the EOUT bit asserted (see below) *if* the accumulated energy is negative.

EOUT — Indicates that enough positive/negative energy has been reached within the internal $\overline{\text{EOUT}}$ Energy Accumulation Register (not accessible to user) to mandate the generation of one or more pulses on the $\overline{\text{EOUT}}$ pin (if enabled, see *Configuration Register*). The energy flow may indicate negative energy or positive energy. (The sign is determined by the EDIR bit, described above). This EOUT bit is cleared automatically when the energy rate drops below the level that produces a 4 kHz EOUT pin rate. The bit can also be cleared by writing to the Status Register. This status bit is set with a maximum frequency of 4 kHz (when MCLK/K is 4.096 MHz). When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate by a factor of 4.096 MHz / (MCLK/K) to get the actual pulse-rate.

DRDY — Data Ready. When running in 'single computation cycle' or 'continuous computation cycles' data acquisition modes, this bit will indicate the end of computation cycles. When running calibrations, this bit indicates that the calibration sequence has completed, and the results have been stored in the offset or gain registers.

5.12 Control Register

Address: 28

23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Res	Res	Res	Res	Res	Res	Res	STOP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	MECH	Res	INTL	SYNC	NOCPU	NOOSC	STEP

Default** = 0x000000

STOP — 1 = used to terminate the new EEBOOT sequence.

Res — Reserved. These bits must be set to zero.

MECH — 1 = widens $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses for mechanical counters.

INTL — 1 = converts the $\overline{\text{INT}}$ output to open drain configuration.

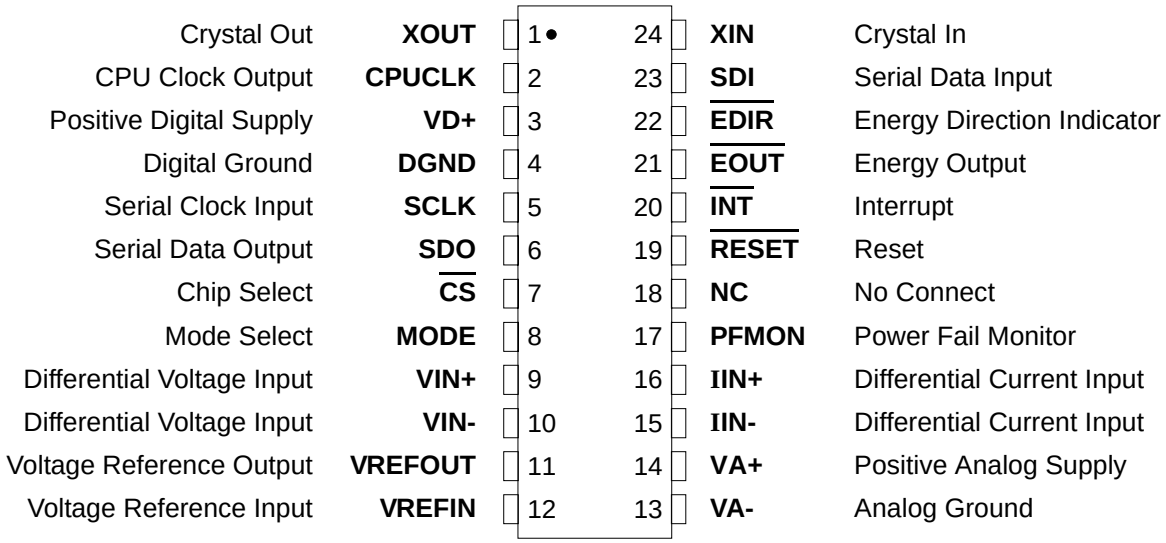
SYNC — 1 = forces internal A/D converter clock to synchronize to the initiation of a conversion command.

NOCPU — 1 = converts the CPUCLK output to a one-bit output port. Reduces power consumption.

NOOSC — 1 = saves power by disabling the crystal oscillator for external drive.

STEP — 1 = enables stepper-motor signals on the $\overline{\text{EOUT}}$/$\overline{\text{EDIR}}$ pins.

6. PIN DESCRIPTIONS

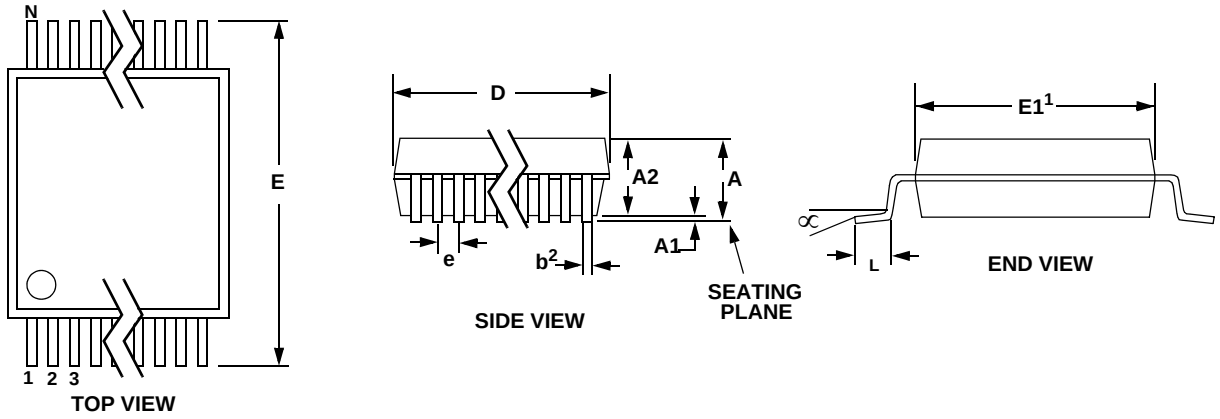


Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible clock) can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK -** A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
Serial Data Output	6	**SDO -** SDO is the output pin of the serial data port. Its output will be in a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$ -** When low, the port will recognize SCLK. An active high on this pin forces the SDO pin to a high impedance state. $\overline{CS}$ should be changed when SCLK is low.
Mode Select	8	**MODE** - When at logic high, the CS5460A can perform the auto-boot sequence with the aid of an external serial EEPROM to receive commands and settings. When at logic low, the CS5460A assumes normal “host mode” operation. This pin is pulled down to logic low if left unconnected, by an internal pull-down resistor to DGND.
Interrupt	20	**$\overline{INT}$ -** When $\overline{INT}$ goes low it signals that an enabled event has occurred. $\overline{INT}$ is cleared (logic 1) by writing the appropriate command to the CS5460A.
Energy Output	21	**$\overline{EOUT}$ -** The energy output pin output a fixed-width pulse rate output with a rate (programmable) proportional to real (billable) energy.
Energy Direction Indicator	22	**$\overline{EDIR}$** - The energy direction indicator indicates if the measured energy is negative.
Serial Data Input	23	**SDI -** the input pin of the serial data port. Data will be input at a rate determined by SCLK.
Measurement and Reference Input		
Differential Voltage Inputs	9,10	**VIN+, VIN- -** Differential analog input pins for voltage channel.

Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 V and is reference to the VA- pin on the converter.
Voltage Reference Input	12	**VREFIN -** The voltage input to this pin establishes the voltage reference for the on-chip modulator.
Differential Current Inputs	15,16	**IIN+, IIN- -** Differential analog input pins for current channel.
Power Supply Connections		
Positive Digital Supply	3	**VD+ -** The positive digital supply is nominally +5 V ±10% relative to DGND.
Digital Ground	4	**DGND -** The common-mode potential of digital ground must be equal to or above the common-mode potential of VA-.
Negative Analog Supply	13	**VA- -** The negative analog supply pin must be at the lowest potential.
Positive Analog Supply	14	**VA+ -** The positive analog supply is nominally +5 V ±10% relative to VA-.
Power Fail Monitor	17	**PFMON -** The power fail Monitor pin monitors the analog supply. Typical threshold level (PMLO) is 2.45 V with respect to the VA- pin. If PFMON voltage threshold is tripped, the LSD (low-supply detect) bit is set in the Status Register. Once the LSD bit has been set, it will not be able to be reset until the PFMON voltage increases ~100 mV (typical) above the PMLO voltage. Therefore, there is hysteresis in the PFMON function.
$\overline{\text{RESET}}$	19	**Reset -** When reset is taken low, all internal registers are set to their default states.
Other		
No Connection	18	**NC -** No connection. Pin should be left floating.

7. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

8. ORDERING INFORMATION

Model	Temperature	Package
CS5460A-BSZ (lead free)	-40 to +85 °C	24-pin SSOP

9. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5460A-BSZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

10. REVISION HISTORY

Revision	Date	Changes
F2	September 2004	Added Lead Free part numbers
F3	August 2005	Updated legal notice.
F4	November 2007	Changed PSSR for voltage channel from 48 dB min. to 65 dB typical.
F5	April 2011	Removed lead-containing (Pb) device ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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