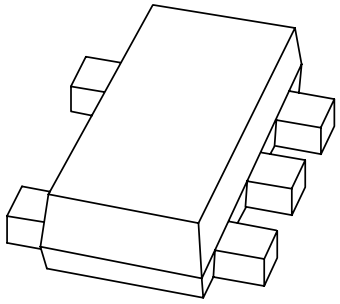
DATA SHEET



BZA900AVL series
Quadruple low capacitance ESD suppressor

Product data sheet
Supersedes data of 2003 Apr 15

2003 Oct 20

NXP founded by Philips

Quadruple low capacitance ESD suppressor

BZA900AVL series

FEATURES

- Low diode capacitance
- Low leakage current
- SOT665 surface mount package
- Common anode configuration.

APPLICATIONS

- Communication systems
- Computers and peripherals
- Audio and video equipment.

DESCRIPTION

Monolithic transient voltage suppressor diode in a five lead SOT665 package for 4-bit wide ESD transient suppression.

MARKING

TYPE NUMBER	MARKING CODE
BZA956AVL	V3
BZA962AVL	V2
BZA968AVL	V1

PINNING

PIN	DESCRIPTION
1	cathode 1
2	common anode
3	cathode 2
4	cathode 3
5	cathode 4

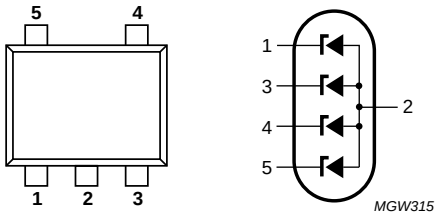


Fig.1 Simplified outline (SOT665) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BZA956AVL	–	plastic surface mounted package; 5 leads	SOT665
BZA962AVL	–	plastic surface mounted package; 5 leads	SOT665
BZA968AVL	–	plastic surface mounted package; 5 leads	SOT665

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
I_Z	working current	T_{amb} = 25 °C	–	note 1	mA
I_F	continuous forward current	T_{amb} = 25 °C	–	200	mA
I_{FSM}	non-repetitive peak forward current	t_p = 1 ms; square pulse	–	3.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 2; see Fig.5	–	335	mW
P_{ZSM}	non repetitive peak reverse power dissipation	square pulse; t_p = 1 ms	–	6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
ESD	electrostatic discharge	IEC 61000-4-2 (contact discharge)	15	–	kV
		HBM MIL-Std 883	10	–	kV

Notes

1. DC working current limited by $P_{tot(max)}$.
2. Device mounted on standard printed-circuit board.

ESD STANDARDS COMPLIANCE

STANDARD	CONDITIONS
IEC 61000-4-2, level 4 (ESD)	>15 kV (air); >8 kV (contact discharge)
HBM MIL-Std 883, class 3	>4 kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	all diodes loaded	370	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to solder point; note 1	one diode loaded	135	K/W
		all diodes loaded	125	K/W

Note

1. Solder point of common anode (pin 2).

ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	forward voltage	I_F = 200 mA	–	–	1.2	V
I_R	reverse current					
	BZA956AVL	V_R = 3 V	–	–	200	nA
	BZA962AVL	V_R = 4 V	–	–	100	nA
	BZA968AVL	V_R = 4.3 V	–	–	20	nA
V_Z	working voltage	I_Z = 1 mA				
	BZA956AVL		5.32	5.6	5.88	V
	BZA962AVL		5.89	6.2	6.51	V
	BZA968AVL		6.46	6.8	7.14	V
r_{dif}	differential resistance	I_Z = 1 mA				
	BZA956AVL		–	–	200	Ω
	BZA962AVL		–	–	150	Ω
	BZA968AVL		–	–	100	Ω
S_Z	temperature coefficient	I_Z = 1 mA				
	BZA956AVL		–	1.3	–	mV/K
	BZA962AVL		–	2.4	–	mV/K
	BZA968AVL		–	2.9	–	mV/K
C_d	diode capacitance	f = 1 MHz; V_R = 0				
	BZA956AVL		–	22	28	pF
	BZA962AVL		–	18	22	pF
	BZA968AVL		–	16	19	pF
	diode capacitance	f = 1 MHz; V_R = 5 V				
	BZA956AVL		–	12	17	pF
	BZA962AVL		–	9	12	pF
	BZA968AVL		–	8	11	pF
I_{ZSM}	non-repetitive peak reverse current	t_p = 1 ms; T_{amb} = 25 °C				
	BZA956AVL		–	–	0.90	A
	BZA962AVL		–	–	0.85	A
	BZA968AVL		–	–	0.80	A

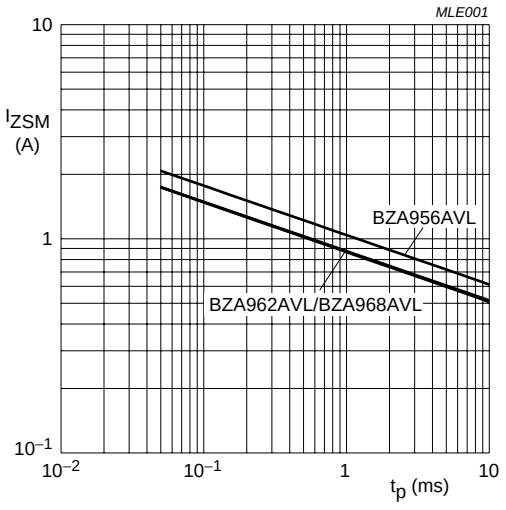


Fig.2 Maximum non-repetitive peak reverse current as a function of pulse time.

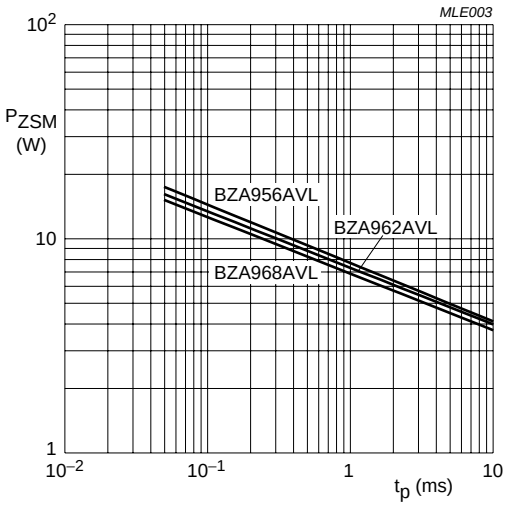
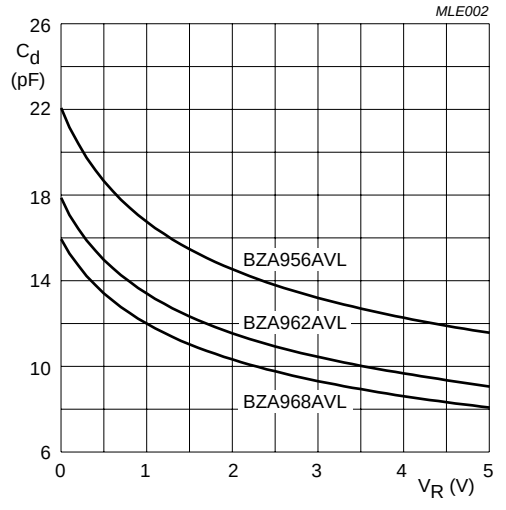


Fig.3 Maximum non-repetitive peak reverse power dissipation as a function of pulse duration (square pulse).



T_j = 25 °C; f = 1 MHz.

Fig.4 Diode capacitance as a function of reverse voltage; typical values.

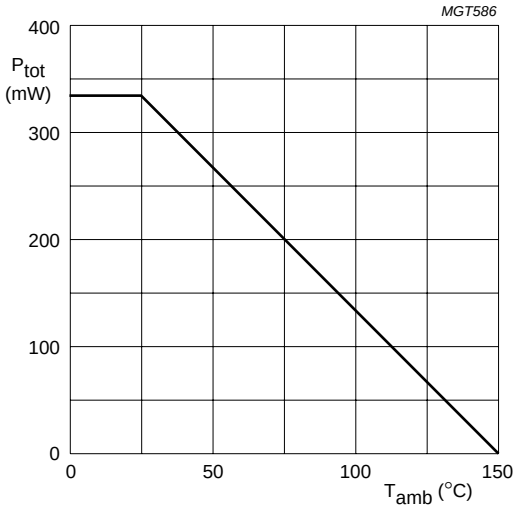
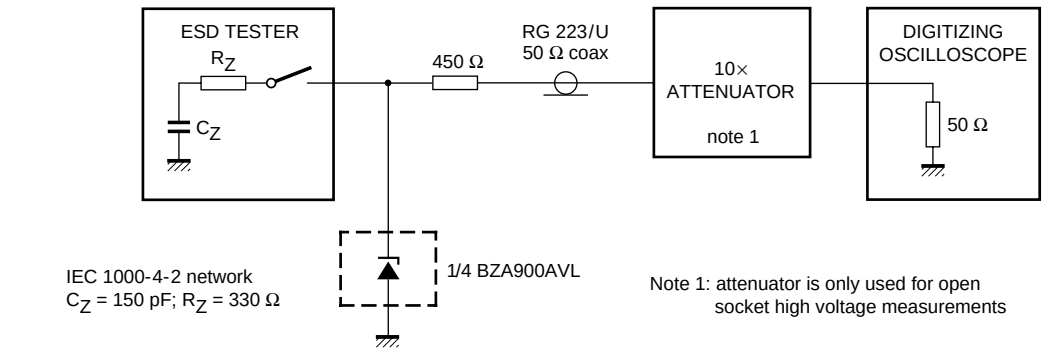
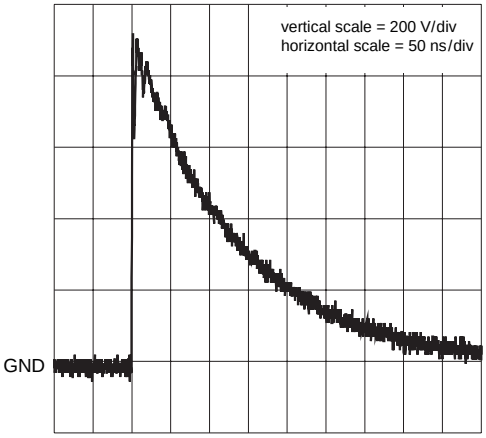
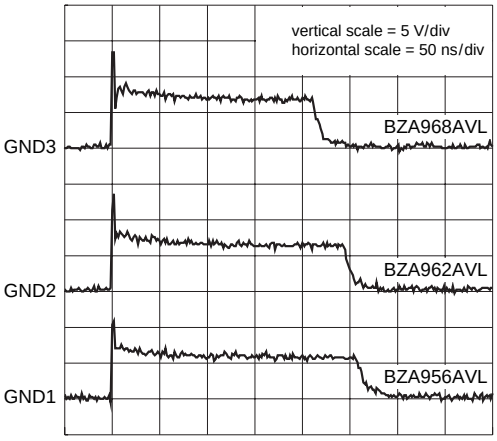


Fig.5 Power derating curve.

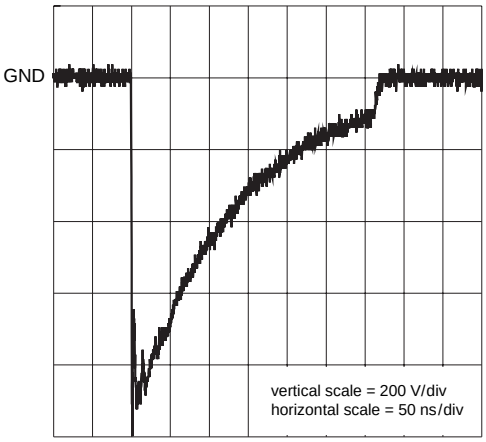




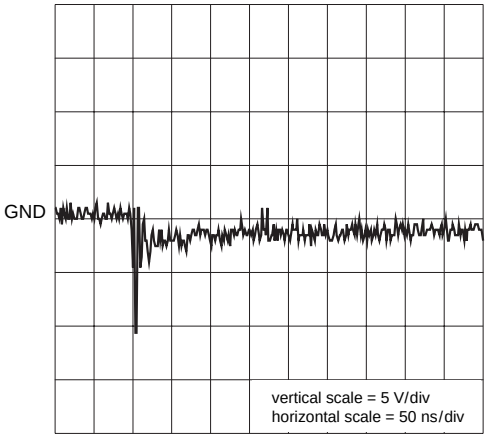
unclamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



unclamped −1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped −1 kV ESD voltage waveform (IEC 1000-4-2 network)

MLE005

Fig.6 ESD clamping test set-up and waveforms.

APPLICATION INFORMATION

Typical common anode application

A quadruple transient suppressor in a SOT665 package makes it possible to protect four separate lines using only one package. Two simplified examples are shown in Figs.7 and 8.

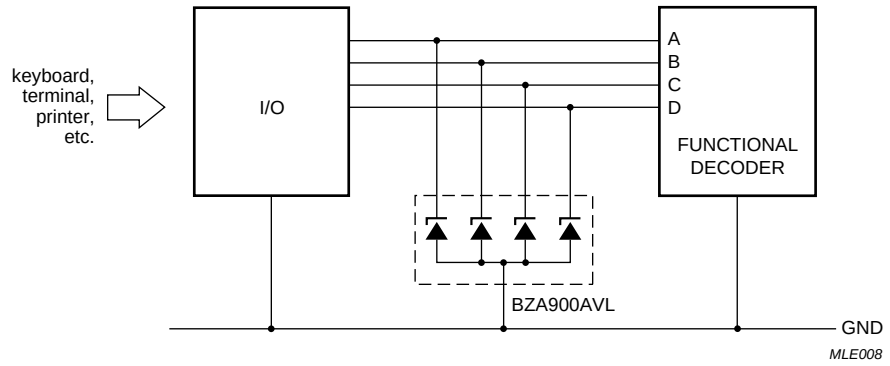


Fig.7 Computer interface protection.

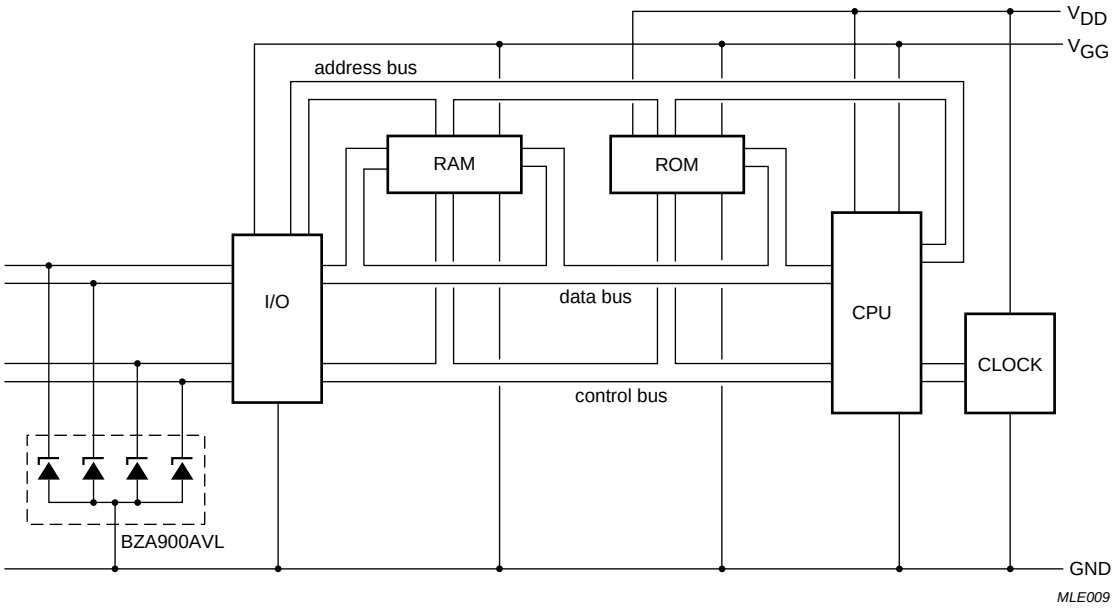


Fig.8 Microprocessor protection.

Device placement and printed-circuit board layout

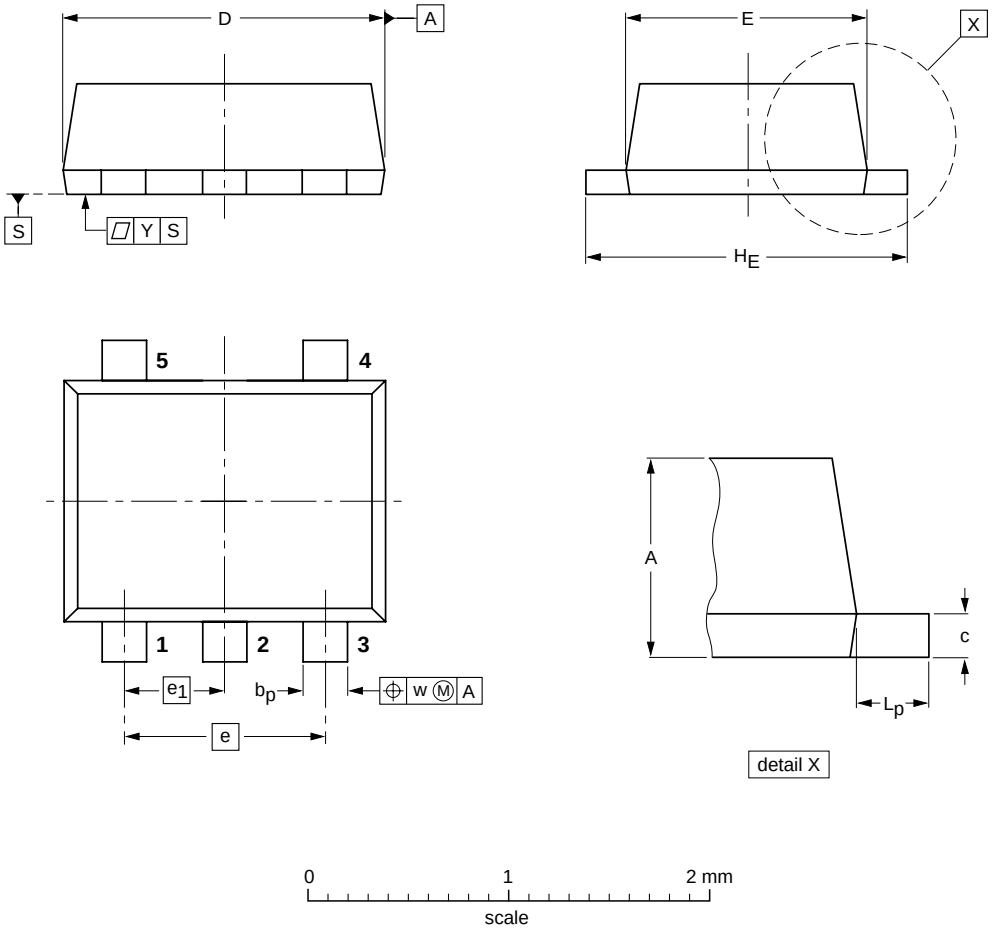
Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA900AVL is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage (V = L di/dt) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors
2. Keep parallel signal paths to a minimum
3. Avoid running protection conductors in parallel with unprotected conductors
4. Minimize all printed-circuit board loop areas including power and ground loops
5. Minimize the length of the transient return path to ground
6. Avoid using shared transient return paths to a common ground point.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT665**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT665						~~01-01-04~~ 01-08-27

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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