Features

- **16 Mbit SRAM Multi Chip Module**
- **Allows 32-, 16- or 8-bit access configuration**
- **Operating Voltage: 3.3V ± 0.3V, 5V Tolerant**
- **Access Time:**
  - **25 ns**
  - **20 ns**
  - **18 ns (preliminary information)**
- **Very Low Power Consumption**
  - **Active: 595 mW per byte (Max) @ 20 ns(1), 415mW per byte (Max) @ 50ns(2)**
  - **Standby: 15 mW (Typ)**
- **Military Temperature Range: -55 to +125·C**
- **TTL-Compatible Inputs and Outputs**
- **Asynchronous**
- **Die manufactured on Atmel 0.25 µm Radiation Hardened Process**
- **No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm²@125°C**
- **Tested up to a Total Dose of 300 krads (Si) according to MIL-STD-883 Method 1019**
- **ESD better than 2000V**
- **Quality Grades:**
  - **QML-Q or V**
  - **ESCC**
- **950 Mils Wide MQFPT68 Package**
- **Mass : 8.5 grams**

Notes: 1. For AT68166HT-20 only. 540mW for AT68166HT-25.
2. For AT68166HT-20 only. 450mW for AT68166HT-25.

Description

The AT68166HT is a 16Mbit SRAM packaged in a hermetic Multi Chip Module (MCM) for space applications.

The AT68166HT MCM incorporates four 4Mbit AT60142HT SRAM dice. It can be organized as either one bank of 512Kx8, two banks of 512Kx16 or four banks of 512Kx8. It combines rad-hard capabilities, a latch-up threshold of 80MeV.cm²/mg, a Multiple Bit Upset immunity and a total dose tolerance of 300Krads, with a fast access time.

The MCM packaging technology allows a reduction of the PCB area by 50% with a weight savings of 75% compared to four 4Mbit packages.

Thanks to the small size of the 4Mbit SRAM die, Atmel has been able to accommodate the assembly of the four dice on one side of the package which facilitates the power dissipation.

The compatibility with other products allows designers to easily migrate to the Atmel AT68166HT memory.

The AT68166HT is powered at 3.3V and is 5V tolerant.

The AT68166HT is processed according to the test methods of the latest revision of the MIL-PRF-38535 or the ESCC 9000.

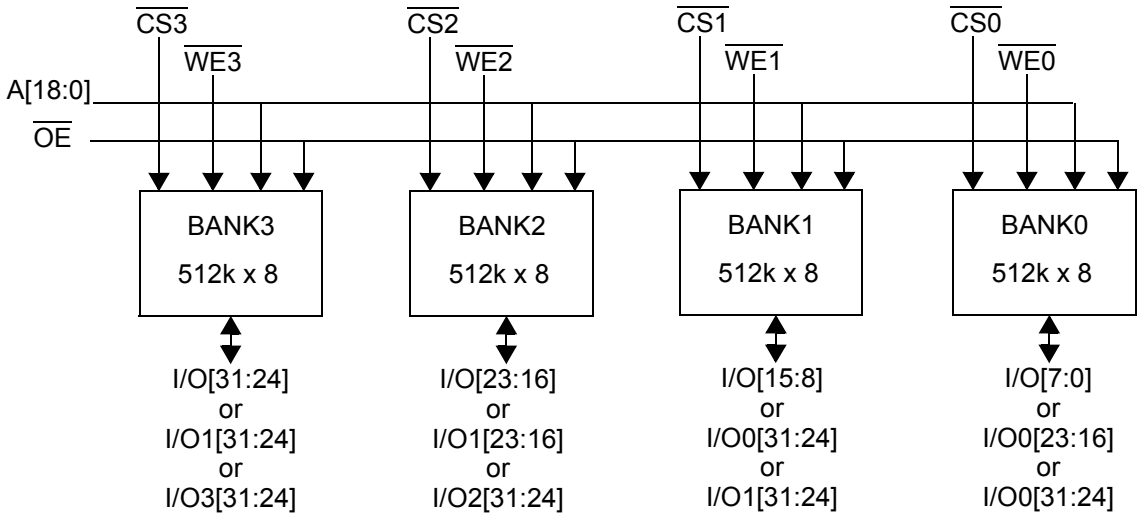
Rad Hard 16 MegaBit 3.3V 5V Tolerant SRAM Multi-Chip Module

AT68166HT

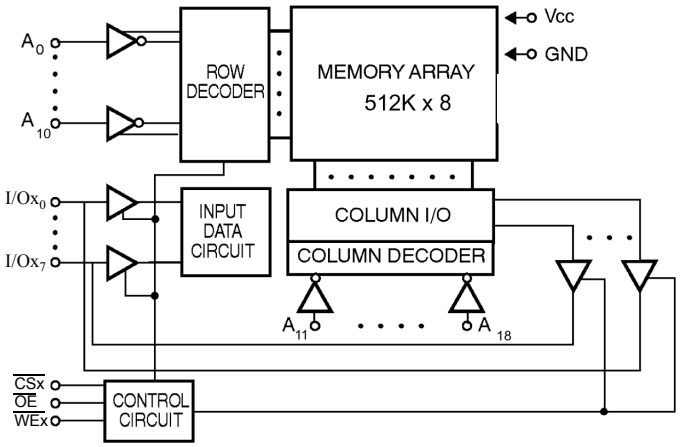
7843D–AERO–11/13

Block Diagram

AT68166HT Block Diagram



512K x 8 Banks Block Diagram (AT60142HT)



Pin Configuration

AT68166HT is packaged in a MQFPT68. The pin assignment depends on the access time.

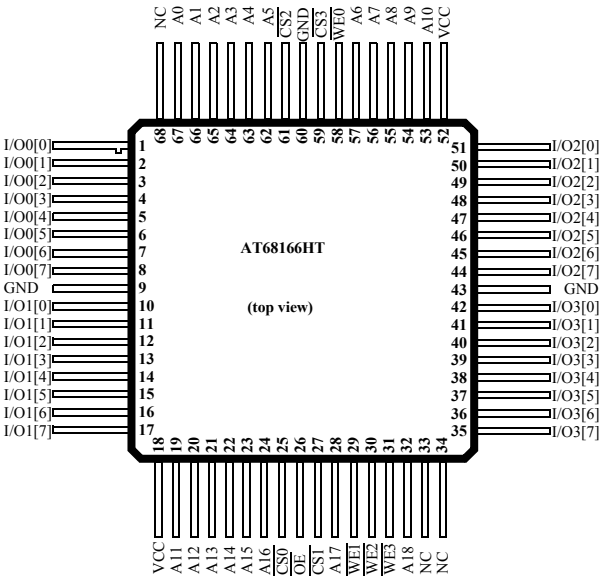
There are 2 versions as described in the table below :

Access Time	25 ns	20 ns	18 ns
Package Version	YM	YS	YS

Table 1. Pin assignment for YS & YM versions

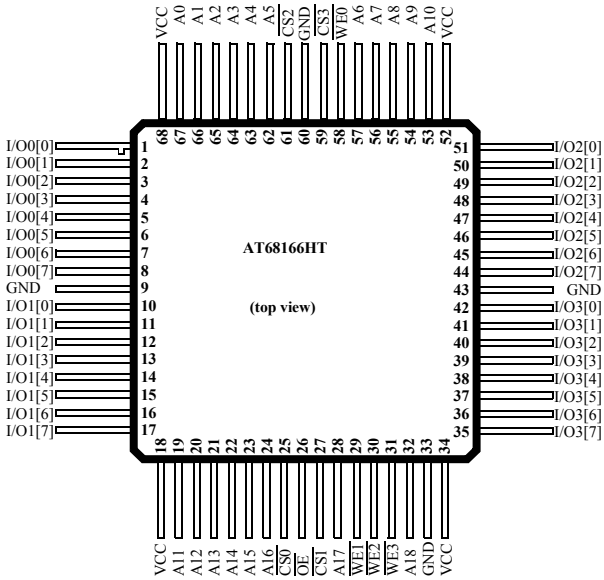
Lead	Signal	Lead		Signal	Lead	Signal	Lead		Signal
1	I/O0[0]	18		VCC	35	I/O3[7]	52		VCC
2	I/O0[1]	19		A11	36	I/O3[6]	53		A10
3	I/O0[2]	20		A12	37	I/O3[5]	54		A9
4	I/O0[3]	21		A13	38	I/O3[4]	55		A8
5	I/O0[4]	22		A14	39	I/O3[3]	56		A7
6	I/O0[5]	23		A15	40	I/O3[2]	57		A6
7	I/O0[6]	24		A16	41	I/O3[1]	58		$\overline{WE0}$
8	I/O0[7]	25		$\overline{CS0}$	42	I/O3[0]	59		$\overline{CS3}$
9	GND	26		$\overline{OE}$	43	GND	60		GND
10	I/O1[0]	27		$\overline{CS1}$	44	I/O2[7]	61		$\overline{CS2}$
11	I/O1[1]	28		A17	45	I/O2[6]	62		A5
12	I/O1[2]	29		$\overline{WE1}$	46	I/O2[5]	63		A4
13	I/O1[3]	30		$\overline{WE2}$	47	I/O2[4]	64		A3
14	I/O1[4]	31		$\overline{WE3}$	48	I/O2[3]	65		A2
15	I/O1[5]	32		A18	49	I/O2[2]	66		A1
16	I/O1[6]	33	YS	GND	50	I/O2[1]	67		A0
			YM	NC					
17	I/O1[7]	34	YS	VCC	51	I/O2[0]	68	YS	VCC
			YM	NC				YM	NC

Figure 1. YM package pin assignment



Note: NC pins are not bonded internally. So, they can be connected to GND or Vcc.

Figure 2. YS package pin assignment



Pin Description

Table 2. Pin Names

Name	Description
A0 - A18	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
$\overline{WE0}$ - $\overline{WE3}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND[1]	Ground

Note: 1. The package lid is connected to GND

Table 3. Truth Table[1]

$\overline{CSx}$	$\overline{WEx}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	Z	Standby
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	Z	Output Disable

Note: 1. L=low, H=high, X= H or L, Z=high impedance.

Electrical Characteristics

Absolute Maximum Ratings*

Supply Voltage to GND Potential:	-0.5V to 4.6V
Voltage range on any input:	GND -0.5V to 7.0V
Voltage range on any ouput:	GND -0.5V to 7.0V
Storage Temperature:	-65·C to +150·C
Output Current from Outputs Pins:	20 mA
Electrostatic Discharge Voltage: (MIL STD 883D Method 3015)	> 2000V

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.**

Military Operating Range

Operating Voltage	Operating Temperature
3.3 ± 0.3V	-55·°C to + 125·°C

Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
Vcc	Supply voltage	3.0	3.3	3.6	V
GND	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	5.5V(1)	V

Note: 1. 5.8V in transient conditions.

Capacitance

Parameter	Description	Min	Typ	Max	Unit
C_{in}(1) (OE and Ax)	Input capacitance	–	–	48	pF
C_{in}(1) (CSx and WEx)	Input capacitance	–	–	12	pF
C_{io}(1)	I/O capacitance	–	–	12	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions **TA = -55°C to + 125°C; Vss = 0V; V_{CC} = 3.0V to 3.6V**

Parameter	Description	Minimum	Typical	Maximum			Unit
				AT68166HT-25	AT68166HT-20	AT68166HT-18	
IIX(1)	Input leakage current	-1	–	1	1	1	µA
IOZ(1)	Output leakage current	-1	–	1	1	1	µA
IIH(2) at 5.5V	Input Leakage Current ($\overline{OE}$ & Axx)	–	–	10	6	6	µA
	Input Leakage Current ($\overline{WE}$ & $\overline{CS}$)	–	–	5	2	2	µA
IOZH(2) at 5.5V	Output Leakage Current	–	–	5	1.5	1.5	µA
VOL(3)	Output low voltage	–	–	0.4	0.4	0.4	V
VOH(4)	Output high voltage	2.4	–	–	–	–	V

Notes:
1. GND < V_{IN} < V_{CC}, GND < V_{OUT} < V_{CC} Output Disabled.
2. V_{IN} = 5.5V, V_{OUT} = 5.5V, Output Disabled.
3. V_{CC} min, - I_{OL} = 6 mA
4. V_{CC} min, I_{OH} = -4 mA

Consumption

Symbol	Description	TAVAV/TAVAW Test Condition	AT68166HT-25	AT68166HT-20	AT68166HT-18 (preliminary)	Unit	Value
I_{CCSB}(1)	Standby Supply Current	–	10	7	7.5	mA	max
I_{CCSB1}(2)	Standby Supply Current	–	8	6	7	mA	max
I_{CCOP}(3) Read per byte	Dynamic Operating Current	18 ns 20 ns 25 ns 50 ns 1 µs	– – 150 85 15	– 165 145 80 12	170 165 145 80 12	mA	max
I_{CCOP}(4) Write per byte	Dynamic Operating Current	18 ns 20 ns 25 ns 50 ns 1 µs	– – 150 125 110	– 140 135 115 105	145 140 135 115 105	mA	max

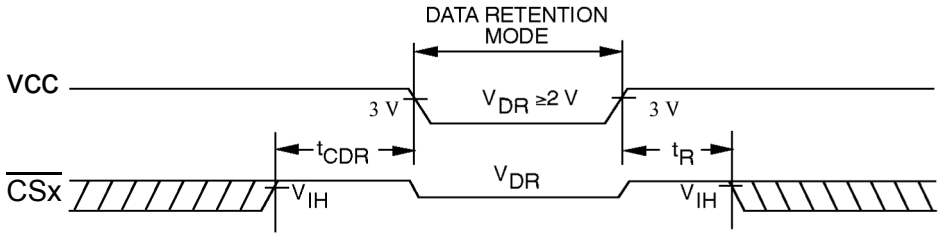
Notes:
1. All $\overline{CSx} \geq V_{IH}$
2. All $\overline{CSx} \geq V_{CC}$ - 0.3V
3. F = $1/_{TAVAV}$, I_{out} = 0 mA, $\overline{WEx}$ = $\overline{OE}$ = V_{IH}, V_{IN} = GND/V_{CC}, V_{CC} max.
4. F = $1/_{TAVAW}$, I_{out} = 0 mA, $\overline{WEx}$ = V_{IL}, $\overline{OE}$ = V_{IH} , V_{IN} = GND/V_{CC}, V_{CC} max.

Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select $\overline{CSx}$ must be held high within V_{CC} to V_{CC} -0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions $\overline{CSx}$ and $\overline{OE}$ must be kept between V_{CC} + 0.3V and 70% of V_{CC}.
4. The RAM can begin operation > t_R ns after V_{CC} reaches the minimum operation voltages (3V).

Figure 3. Data Retention Timing



Data Retention Characteristics

Parameter	Description	Min	Typ T_A = 25·C	Max	Unit
V_{CCDR}	V_{CC} for data retention	2.0	–	–	V
t_{CDR}	Chip deselect to data retention time	0.0	–	–	ns
t_R	Operation recovery time	t_{AVAV} (1)	–	–	ns
I_{CCDR} (2)	Data retention current	–	3	6 (AT68166HT-25)	mA
				4.5 (AT68166HT-20)	
				5 (AT68166HT-18)	

1. T_{AVAV} = Read cycle time.
2. All $\overline{CSx}$ = V_{CC}, V_{IN} = GND/V_{CC}.

AC Characteristics

Test Conditions

Temperature Range: ..... -55 +125 °C

Supply Voltage: ..... 3.3 ±0.3V

Input and Output Timing Reference Levels: 1.5V

Test Loads and Waveforms

Figure 4. Test Loads

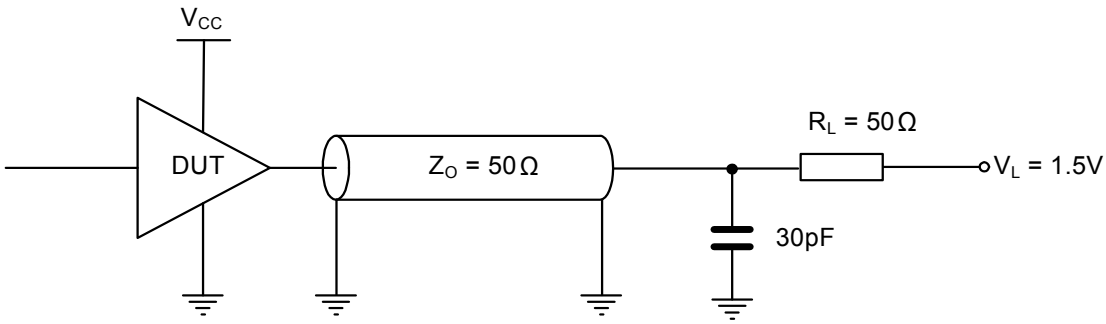


Figure 5. Test Loads specific to TWLQZ, TWHQX, TELQX, TEHQZ, TGLQX, TGHQZ

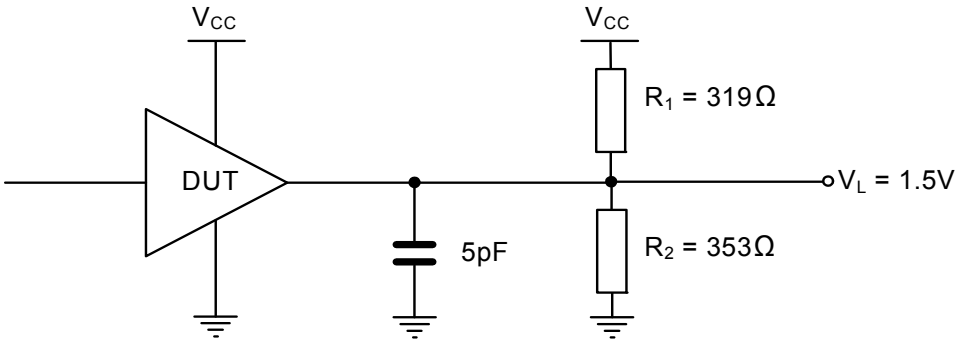
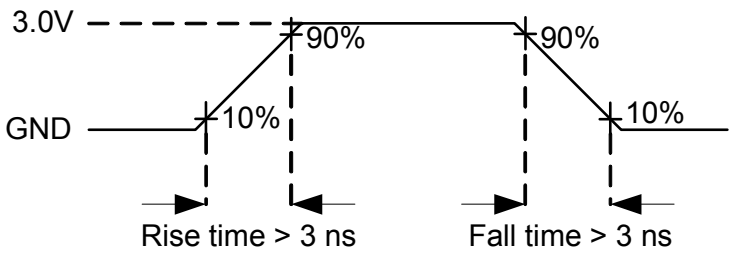


Figure 6. CMOS Input Pulses



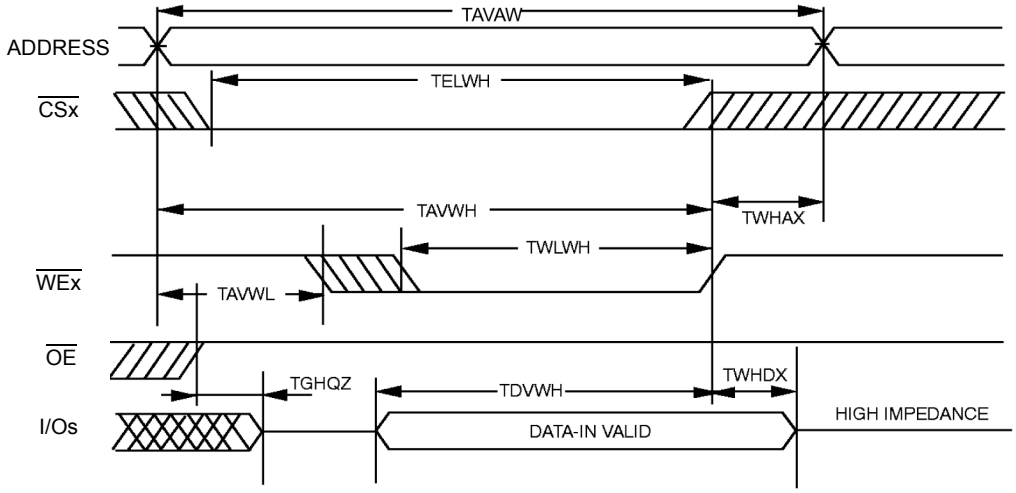
Write Cycle

Table 4. Write cycle timings[1]

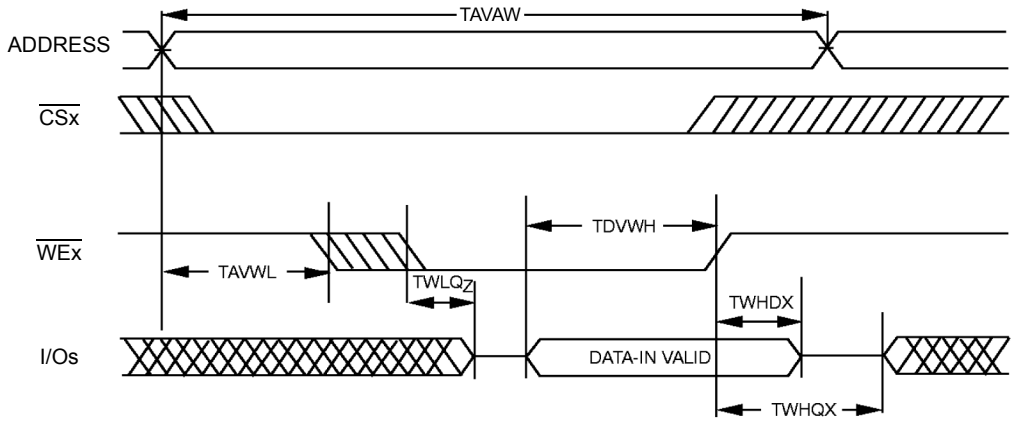
Symbol	Parameter	AT68166HT-25		AT68166HT-20		AT68166HT-18 (preliminary)		Unit
		min	max	min	max	min	max	
TAVAW	Write cycle time	20	-	20	-	18	-	ns
TAVWL	Address set-up time	2	-	2	-	2	-	ns
TAVWH	Address valid to end of write	14	-	11	-	10	-	ns
TDVWH	Data set-up time	9	-	8	-	7	-	ns
TELWH	$\overline{CS}$ low to write end	12	-	12	-	11	-	ns
TWLQZ	Write low to high Z[2]	-	10	-	10	-	9	ns
TWLWH	Write pulse width	12	-	9	-	9	-	ns
TWHAX	Address hold from end of write	0	-	0	-	0	-	ns
TWHDX	Data hold time	2	-	1	-	1	-	ns
TWHQX	Write high to low Z[2]	5	-	5	-	5	-	ns

Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.
2. Parameters guaranteed, not tested, with output loading 5 pF. (See “Test Loads and Waveforms” on page 9.)

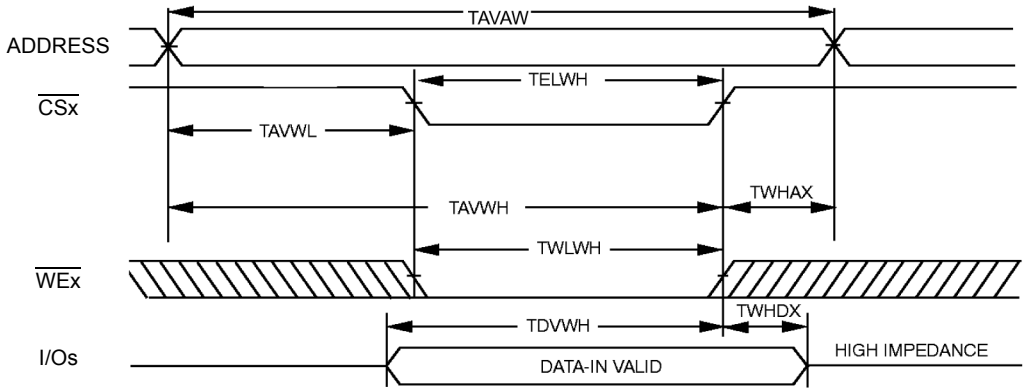
Write Cycle 1. $\overline{WE}$ Controlled, $\overline{OE}$ High During Write



Write Cycle 2. **$\overline{WE}$ Controlled, $\overline{OE}$ Low**



Write Cycle 3. **$\overline{CS}$ Controlled**



Note: The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{WE}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$= V_{IH}.

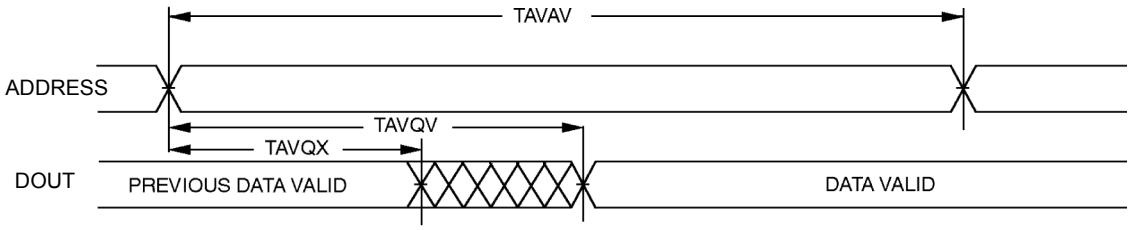
Read Cycle

Table 5. Read cycle timings[1]

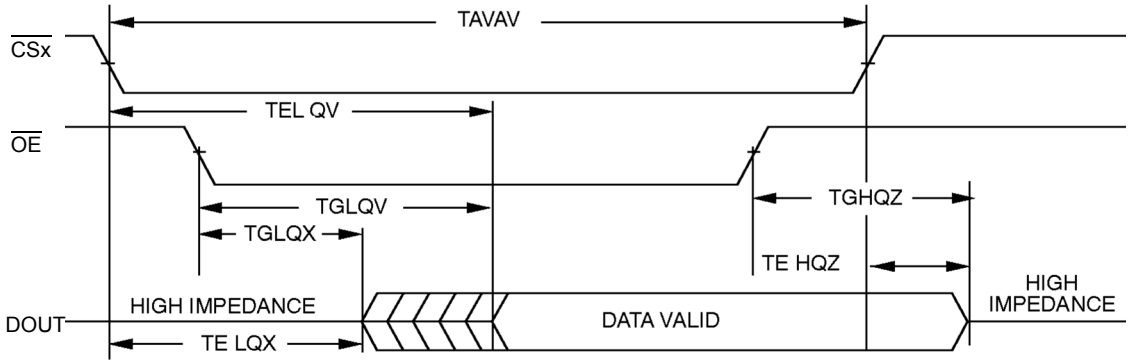
Symbol	Parameter	AT68166HT-25		AT68166HT-20		AT68166HT-18 (preliminary)		Unit
		min	max	min	max	min	max	
TAVAV	Read cycle time	25	-	20	-	18	-	ns
TAVQV	Address access time	-	25	-	20	-	18	ns
TAVQX	Address valid to low Z	5	-	5	-	5	-	ns
TELQV	Chip-select access time	-	25	-	20	-	18	ns
TELQX	$\overline{CS}$ low to low Z[2]	5	-	5	-	5	-	ns
TEHQZ	$\overline{CS}$ high to high Z[2]	-	10	-	9	-	9	ns
TGLQV	Output Enable access time	-	12	-	10	-	9	ns
TGLQX	$\overline{OE}$ low to low Z[2]	2	-	2	-	2	-	ns
TGHQZ	$\overline{OE}$ high to high Z [2]	-	10	-	9	-	9	ns

Notes: 1. Timings figures applicable for 8-bit, 16-bit and 32-bit mode.
2. Parameters guaranteed, not tested, with output loading 5 pF. (See “Test Loads and Waveforms” on page 9.)

Read Cycle 1. **Address Controlled ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})**



Read Cycle 2. **Chip Select Controlled ($\overline{WE}$ = V_{IH})**



Typical Applications

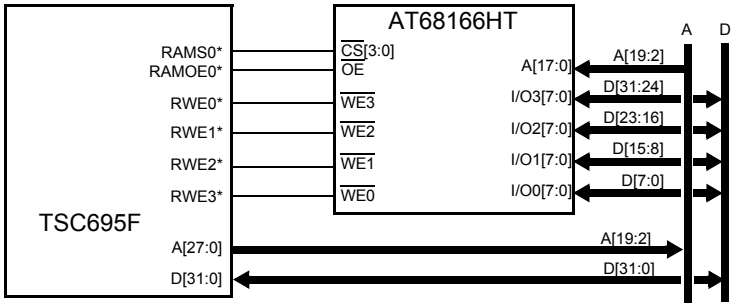
This section shows standard implementations of the AT68166HT in applications.

32-bit mode application

When used on a 32-bit (word) application, the module shall be connected as follow :

- The 32 lines of data are connected to distinct data lines
- The four $\overline{CSx}$ are connected together and linked to a single host $\overline{CS}$ output
- Each of the four $\overline{WE}$x is connected to a dedicated $\overline{WE}$ line on the host to allow byte, half word and word format write.

Figure 7. 32-bit typical application (one SRAM bank)

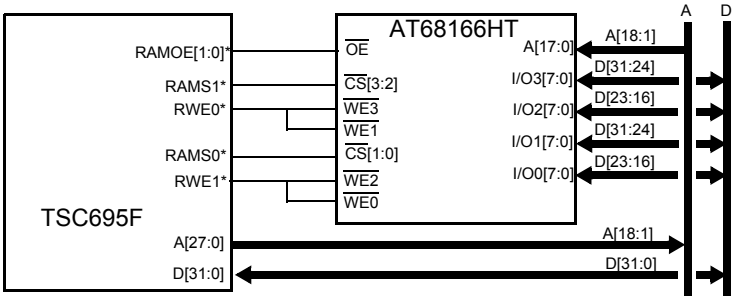


16-bit mode application

When used on a 16-bit (half word) application, the module can be connected as presented in the following figure. This allows the use of a single AT68166HT part for two SRAM memory banks.

All input controls of the AT68166HT not used in the application shall be pulled-up.

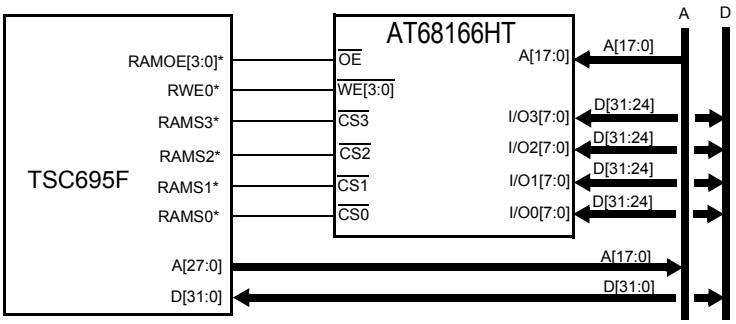
Figure 8. 16-bit typical application (two SRAM banks)



8-bit mode application

When used on a 8-bit (byte) application, the module can be connected as presented in the following figure. This allows the use of a single AT68166HT part for up to four SRAM memory banks. All input controls of the AT68166HT not used in the application shall be pulled-up.

Figure 9. 8-bit typical application (four SRAM banks)



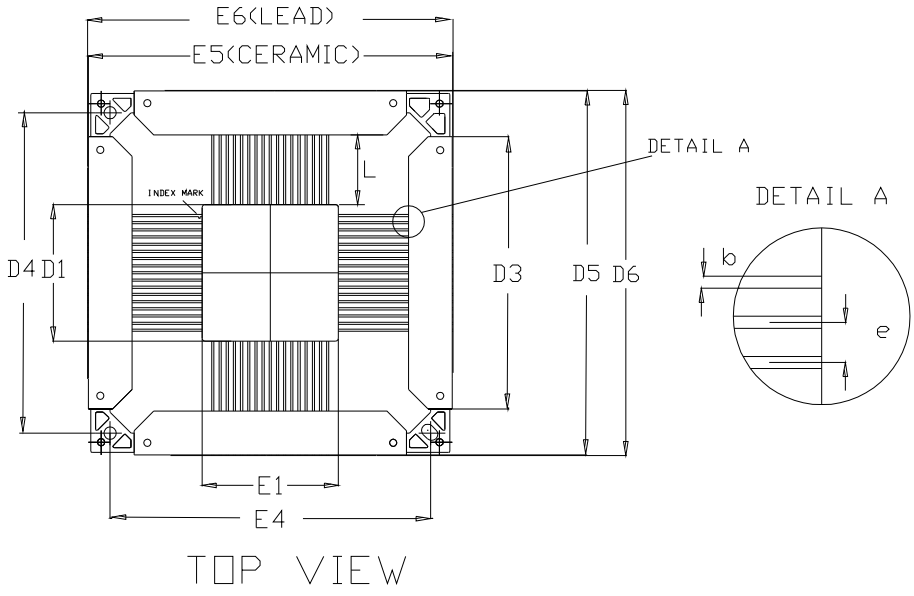
Ordering Information

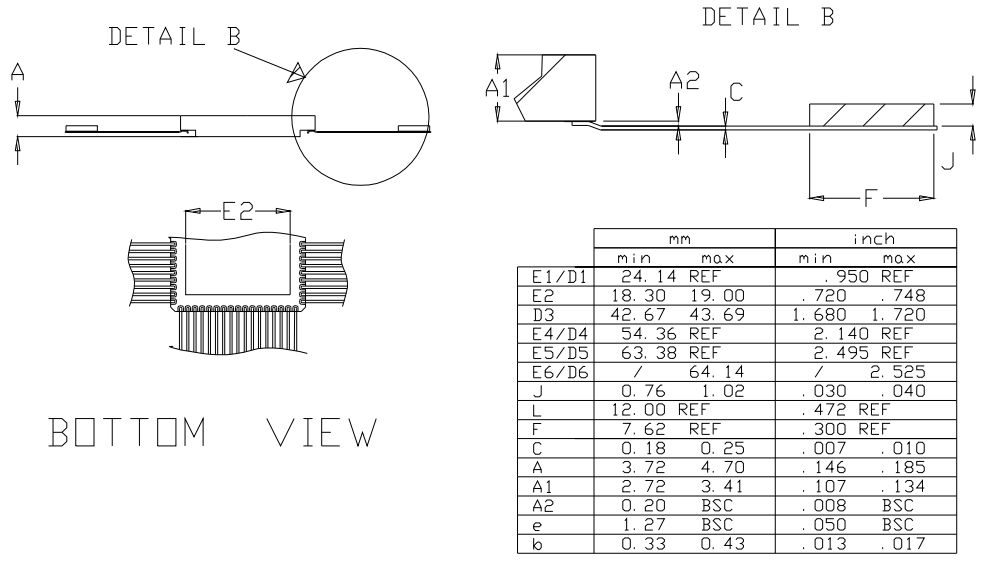
Part Number	Temperature Range	Speed	Package	Flow
AT68166HT-YM25-E	25·C	25 ns	MQFPT68	Engineering Samples
5962-0622907QXC	-55· to +125·C	25 ns	MQFPT68	QML Q
5962-0622907VXC	-55· to +125·C	25 ns	MQFPT68	QML V
5962R0622907VXC	-55· to +125·C	25 ns	MQFPT68	QML V RHA
AT68166HT-YM25-SCC(3)	-55· to +125·C	25 ns	MQFPT68	ESCC
AT68166HT-YS20-E	25·C	20 ns	MQFPT68	Engineering Samples
5962-0622905QYC	-55· to +125·C	20 ns	MQFPT68	QML Q
5962-0622905VYC	-55· to +125·C	20 ns	MQFPT68	QML V
5962R0622905VYC	-55· to +125·C	20 ns	MQFPT68	QML V RHA
AT68166HT-YS20-SCC(3)	-55· to +125·C	20 ns	MQFPT68	ESCC
AT68166HT-YS18-E(1)	25·C	18 ns	MQFPT68	Engineering Samples
AT68166HT-YS18-MQ(1)(2)	-55· to +125·C	18 ns	MQFPT68	Mil Level B
AT68166HT-YS18-SV(1)(2)	-55· to +125·C	18 ns	MQFPT68	Space Level B
AT68166HT-YS18-SR(1)(2)	-55· to +125·C	18 ns	MQFPT68	Space Level B RHA
AT68166HT-YS18-SCC(1)(3)	-55· to +125·C	18 ns	MQFPT68	ESCC

Note:
1. Please contact your local sales office.
2. Will be replaced by SMD part number when available.
3. Will be replaced by ESCC part number when available.

Package Drawing

68-lead Quad Flat Pack (950 Mils) with non conductive tie bar





	mm		inch	
	min	max	min	max
E1/D1	24.14 REF		.950 REF	
E2	18.30	19.00	.720	.748
D3	42.67	43.69	1.680	1.720
E4/D4	54.36 REF		2.140 REF	
E5/D5	63.38 REF		2.495 REF	
E6/D6	/	64.14	/	2.525
J	0.76	1.02	.030	.040
L	12.00 REF		.472 REF	
F	7.62 REF		.300 REF	
C	0.18	0.25	.007	.010
A	3.72	4.70	.146	.185
A1	2.72	3.41	.107	.134
A2	0.20 BSC		.008 BSC	
e	1.27 BSC		.050 BSC	
b	0.33	0.43	.013	.017

Note: 1. Lid is connected to Ground.
2. YM and YS package drawings are identical.

Document Revision History

Creation from AT66168FT without any change.

Changes from Rev. A to Rev. B

Update: “AT68166H Block Diagram”

Update: “Package drawings”

Update: Figures in “Typical applications”

Addition: SMD part-numbers for 20 ns versions (YS package) in “Ordering Information” section

Changes from Rev. B to Rev. C

Update: “AT68166H Block Diagram”

Update: “Package drawings”

Update: Figures in “Typical applications”

Addition: SMD part-numbers for 25 ns versions (YM package) in “Ordering Information” section

Changes from Rev. C to Rev. D

Update: Test Conditions, Test Loads and Waveforms in “AC Characteristics section

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