AT24C04D

I²C-Compatible (2-wire) Serial EEPROM
4-Kbit (512 x 8)

DATASHEET

Features

- Low Voltage Operation
  - V_{CC} = 1.7V to 3.6V
- Internally Organized as 512 x 8 (4K)
- I²C-compatible (2-Wire) Serial Interface
  - 100kHz Standard Mode, 1.7V to 3.6V
  - 400kHz Fast Mode, 1.7V to 3.6V
  - 1MHz Fast Mode Plus (FM+), 2.5V to 3.6V
- Schmitt Triggers, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Write Protect Pin For Full Array Hardware Data Protection
- Ultra Low Active Current (1mA Max) and Standby Current (0.8µA Max)
- 16-byte Page Write Mode
  - Partial Page Writes Allowed
- Random and Sequential Read Modes
- Self-timed Write Cycle within 5ms Max
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Green Package Options (Lead-free/Halide-free/RoHS Compliant)
  - 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN, 8-lead PDIP(1), 5-lead SOT23, and 8-ball VFBGA
- Die Sale Options: Wafer Form and Tape and Reel Available

Description

The Atmel® AT24C04D provides 4,096 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512 words of 8 bits each. The device's cascadable feature allows up to four devices to share a common 2-wire bus. This device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The device is available in space-saving 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN, 8-lead PDIP(1), 5-lead SOT23, and 8-ball VFBGA packages. The entire family of packages operate from 1.7V to 3.6V.

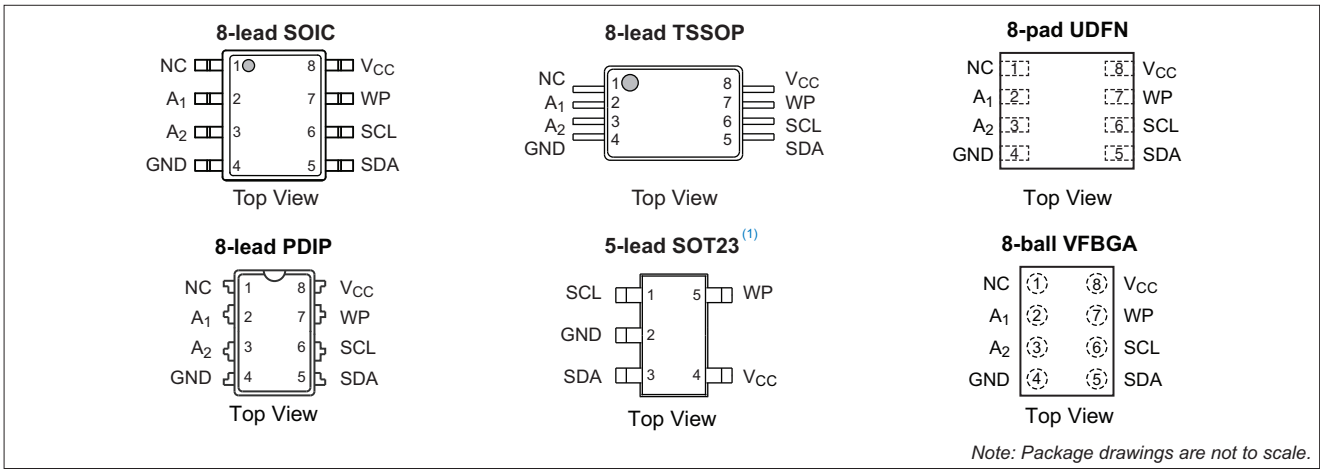
Note: 1. Contact Atmel Sales for the availability of this package.

1. Pin Descriptions and Pinouts

Table 1-1. Pin Descriptions

Pin Number	Pin Symbol	Pin Name and Functional Description	Asserted State	Pin Type
1	NC	**No Connect:** The NC pins are not bonded to a die pad. This pin can be connected to GND or left floating.	—	—
2, 3	A_1, A_2	**Device Address Input:** The A_1 and A_2 pins are used to select the hardware device address and correspond to the sixth and fifth bit of the I^2C seven bit slave address. These pins can be directly connected to V_{CC} or GND, allowing up to four devices on the same bus. Refer to Note 1 for behavior of the pin when not connected.	—	Input
4	GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power
5	SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 10KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
6	SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
7	WP	**Write Protect:** Connecting the WP pin to GND will ensure normal write operations.When the WP pin is connected to VCC, all write operations to the memory are inhibited. Refer to Note 1 for behavior of the pin when not connected.	High	Input
8	V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power

Note: 1. If the A_1, A_2, or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Atmel recommends connecting these pins to a known state whenever possible.



Note: 1. Refer to "Device Addressing" for details about addressing the SOT23 version of the device.

2. Device Block Diagram and System Configuration

Figure 2-1. Block Diagram

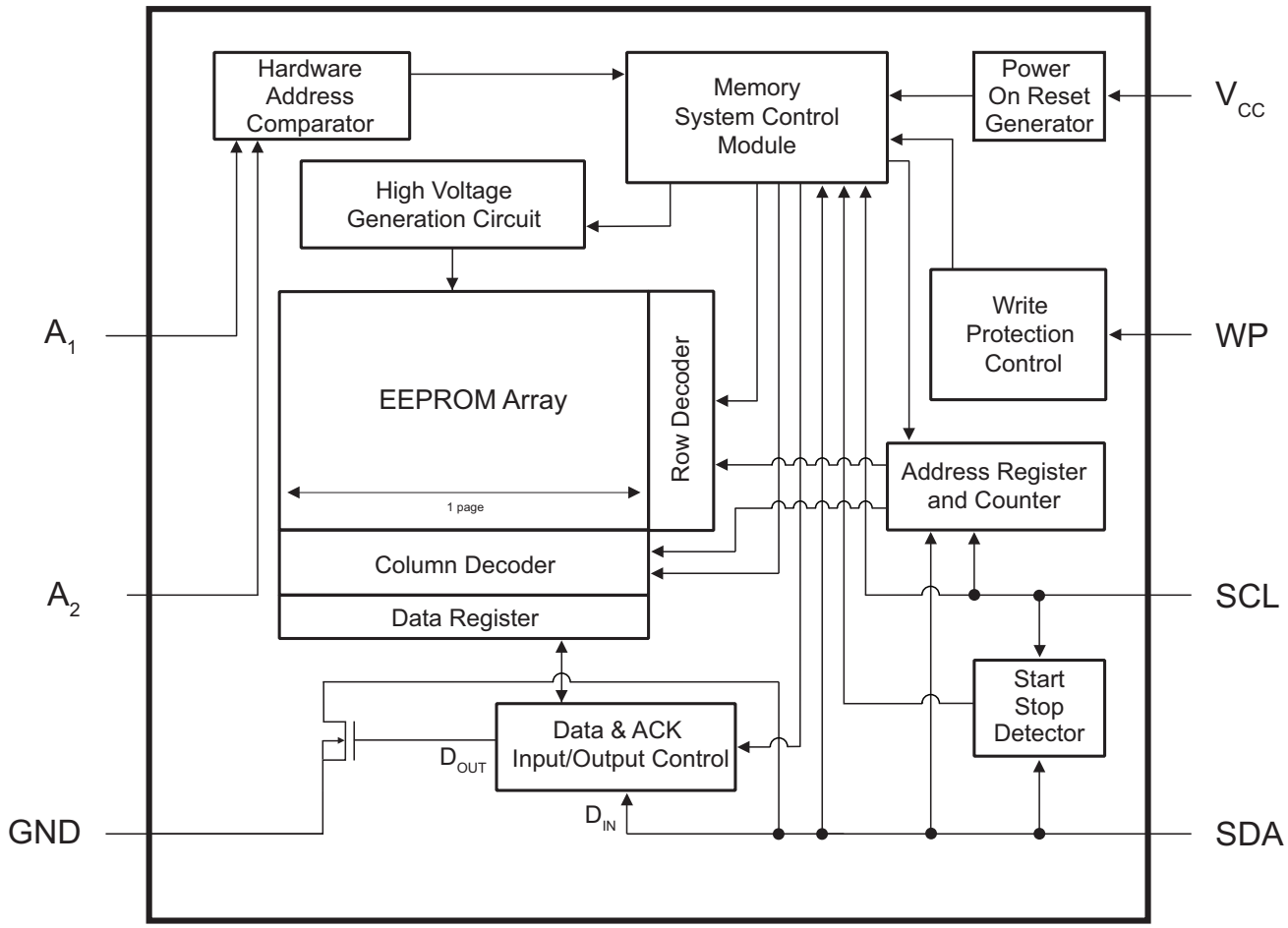
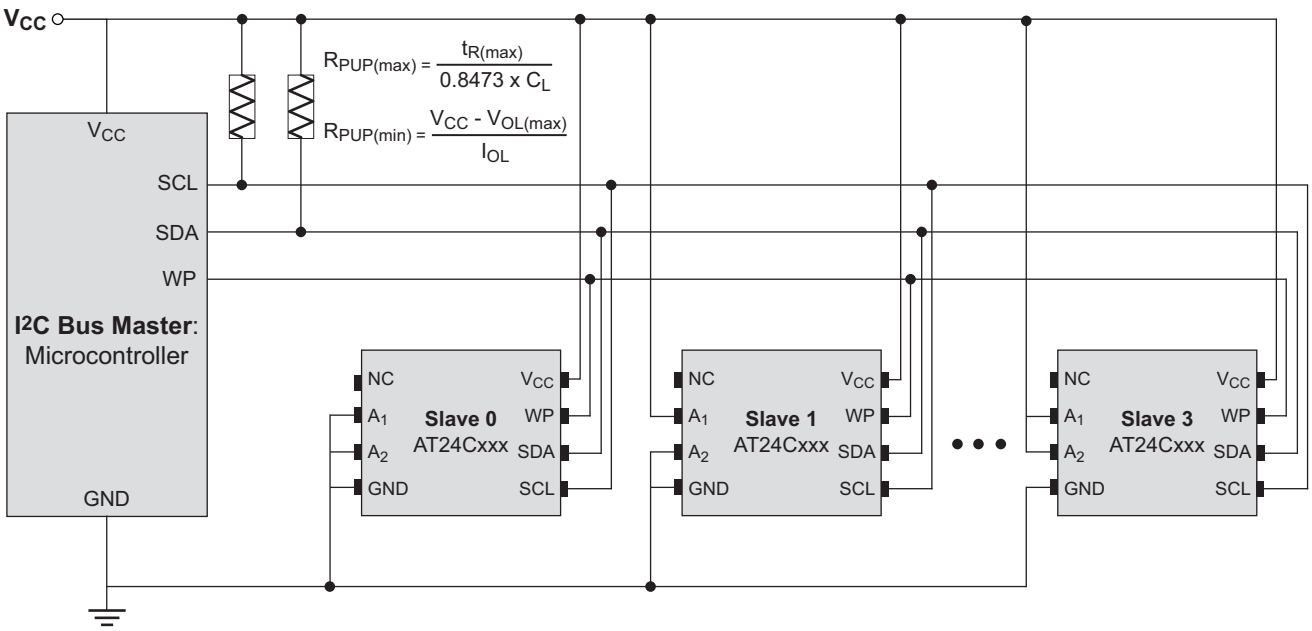


Figure 2-2. System Configuration Using 2-Wire Serial EEPROMs



3. Device Operation and Communication

The AT24C04D operates as a slave device and utilizes a simple I2C-compatible 2-wire digital serial interface to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master as well as to send data back to the Master. Data is always latched into the AT24C04D on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic-high state at the same time.

3.1 Clock and Data Transition Requirements

The SDA pin is an open drain terminal and therefore must be pulled high with an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

3.2 Start and Stop Conditions

3.2.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable Logic 1 state and will bring the device out of standby mode. The Master uses a Start condition to initiate any data transfer sequence, therefore every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Please refer to Figure 3-1 for more details.

3.2.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master can use the Stop condition to end a data transfer sequence with the AT24C04D which will subsequently return to standby mode. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master will perform another operation. Please refer to Figure 3-1 for more details.

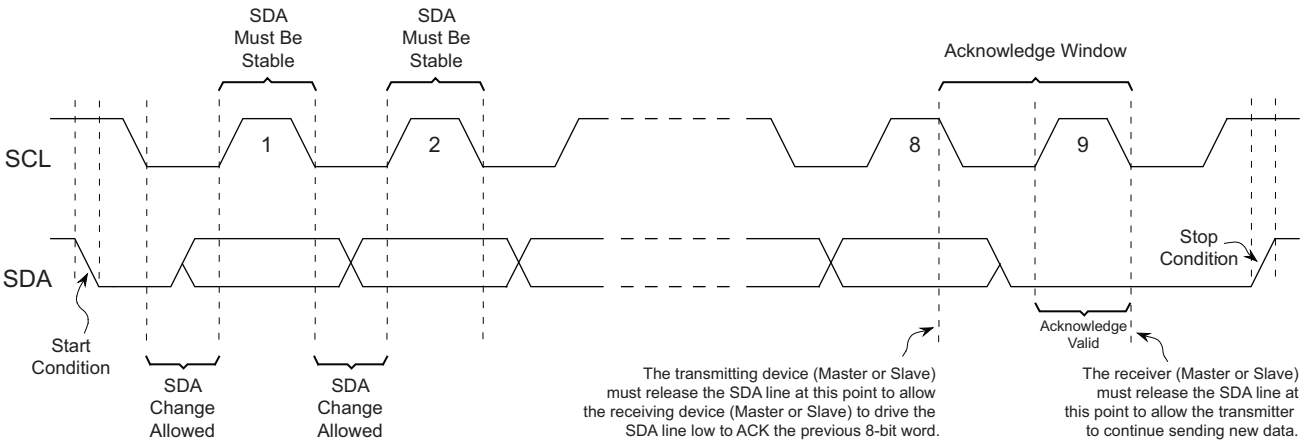
3.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the Master that it has successfully received the data byte by responding with what is known as an acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a Logic 0 during the entire high period of the ninth clock cycle.

When the AT24C04D is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a Logic 1 response to the AT24C04D instead of an ACK response during the ninth clock cycle. This is known as a no-acknowledge (NACK) and is accomplished by the Master sending a Logic 1 during the ninth clock cycle, at which point the AT24C04D will release the SDA line so the Master can then generate a Stop condition.

The transmitting device, which can be the bus Master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a Logic 0 to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 3-1 to better illustrate these requirements.

Figure 3-1. Start Condition, Data Transitions, Stop Condition and Acknowledge



3.4 Standby Mode

The AT24C04D features a low power standby mode which is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Section 8.5, “Power-Up Requirements and Reset Behavior”).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Section 5.).
- At the completion of an internal write cycle (see Section 5., “Write Operations”).
- An unsuccessful match of the device type identifier or hardware address in the Device Address byte occurs (see Section 4.1, “Device Addressing”).
- The bus Master does not ACK the receipt of data read out from the device; instead it sends a NACK response. (see Section 6., “Read Operations”).

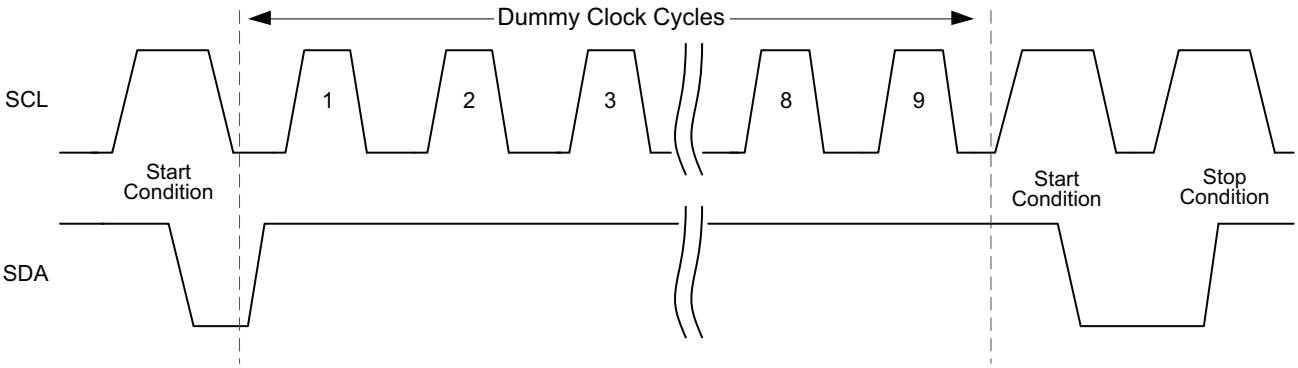
3.5 Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by a Stop condition as seen in Figure 3-2.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Section 8.5.1, “Device Reset”).

Figure 3-2. Software Reset



4. Memory Organization

The AT24C04D is internally organized as 32 pages of 16 bytes each.

4.1 Device Addressing

Accessing the device requires an 8-bit Device Address word following a Start condition to enable the device for a read or write operation. Since multiple slave devices can reside on the serial bus each slave device must have its own unique address so that the Master can access each device independently.

The most significant four bits of the Device Address word is referred to as the device type identifier. The device type identifier `'1010'` (Ah) is required in bits seven through four of the Device Address byte (see Table 4-1).

Following the 4-bit device type identifier are the hardware slave address bits, A_2 and A_1. These bits can be used to expand the address space by allowing up to four 4-Kbit Serial EEPROM devices on the same bus. The A_2 and A_1 values must correlate with the voltage level on the corresponding hardwired input pins A_2 and A_1.

The A_2 and A_1 pins use an internal proprietary circuit that automatically biases it to a Logic 0 state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer's trip point (~0.5 x V_{CC}), the pull-down mechanism disengages. Atmel recommends connecting the A_2 and A_1 pins to a known state whenever possible.

When using the SOT23 package, the A_2 and A_1 pins are not accessible and are left floating. The previously mentioned automatic pull-down circuit will set these pins to a Logic 0 state. As a result, to properly communicate with the device in the SOT23 packages, the A_2 and A_1 software bits must always be set to Logic 0 for any operation.

Following the A_2 and A_1 hardware slave address bits is bit A8 (bit 1 of the Device Address byte), which is the most significant bit of the memory array word address. Please refer to Table 4-1 to review these bit positions.

The eighth bit (bit 0) of the Device Address byte is the Read/Write operation select bit. A Read operation is initiated if this bit is high and a Write operation is initiated if this bit is low.

Upon the successful comparison of the Device Address byte, the EEPROM will return an ACK. If a valid comparison is not made, the device will NACK and return to a standby state.

Table 4-1. Device Address Byte

Package	Device Type Identifier				Hardware Slave Address Bit		MSB of the Word Address	Read/ Write
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, UDFN, PDIP, VFBGA	1	0	1	0	A_2	A_1	A8	R/$\overline{W}$
SOT23	1	0	1	0	0	0	A8	R/$\overline{W}$

For all operations except the Current Address Read, a Word Address byte must be transmitted to the device immediately following the Device Address byte. The Word Address byte consists of the remaining eight bits of the 9-bit memory array word address, and is used to specify which byte location in the EEPROM to start reading or writing. Please refer to Table 4-2 to review these bit positions.

Table 4-2. Word Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A7	A6	A5	A4	A3	A2	A1	A0

The relationship of the AC timing parameters with respect to SCL and SDA for the AT24C04D are shown in the timing waveform Figure 8-1 on page 15. The AC timing characteristics and specifications are outlined in Section 8.4 “AC Characteristics” on page 15.

5. Write Operations

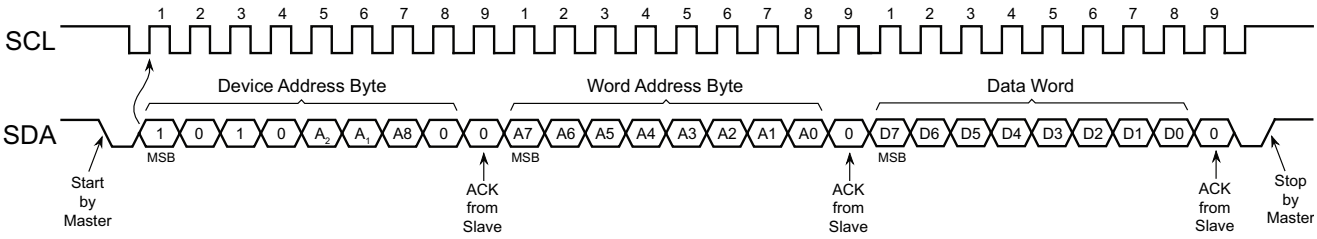
All Write operations for the AT24C04D begin with the Master sending a Start condition, followed by a Device Address byte with the R/W bit set to '0', and then by the Word Address byte. The data value(s) to be written to the device immediately follow the Word Address byte.

5.1 Byte Write

The AT24C04D supports the writing of single 8-bit bytes. Selecting a data word in the AT24C04D requires a 9-bit word address.

Upon receipt of the proper Device Address and Word Address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an Acknowledge. The addressing device, such as a bus Master, must then terminate the Write operation with a Stop condition. At that time the EEPROM will enter an internally self-timed write cycle, which will be completed within t_{WR}, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle, and the EEPROM will not respond until the Write is complete.

Figure 5-1. Byte Write



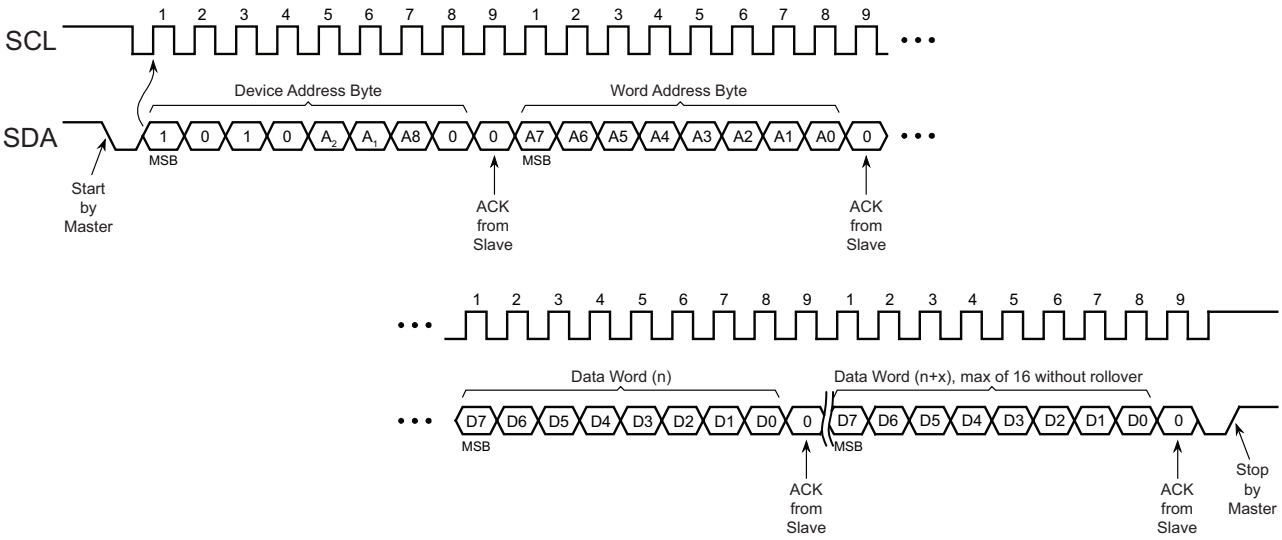
5.2 Page Write

A Page Write operation allows up to 16 bytes to be written in the same write cycle, provided all bytes are in the same row of the memory array (where address bits A8 through A4 are the same). Partial Page Writes of less than 16 bytes are also allowed.

A Page Write is initiated the same way as a Byte Write, but the bus Master does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus Master can transmit up to fifteen additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus Master must issue a Stop condition (see Figure 5-2) at which time the internally self-timed write cycle will begin.

The lower four bits of the word address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page Write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will “roll over” to the beginning of the same page. Nevertheless, creating a roll over event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 5-2. Page Write

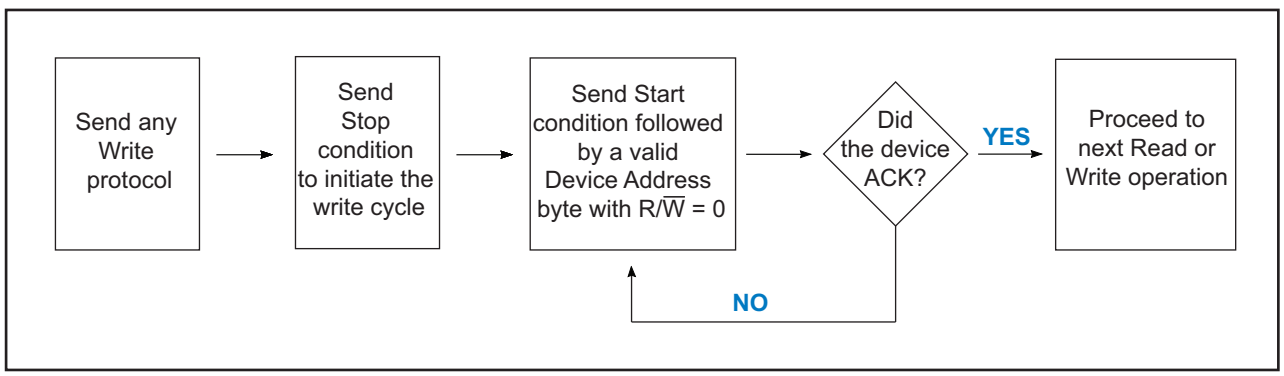


5.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}). This method allows the application to know immediately when the Serial EEPROM write cycle has completed, so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid Device Address byte with the R/$\overline{W}$ bit set at Logic 0. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new Read or Write operation to be immediately initiated. A flow chart has been included below in Figure 5-3 to better illustrate this technique.

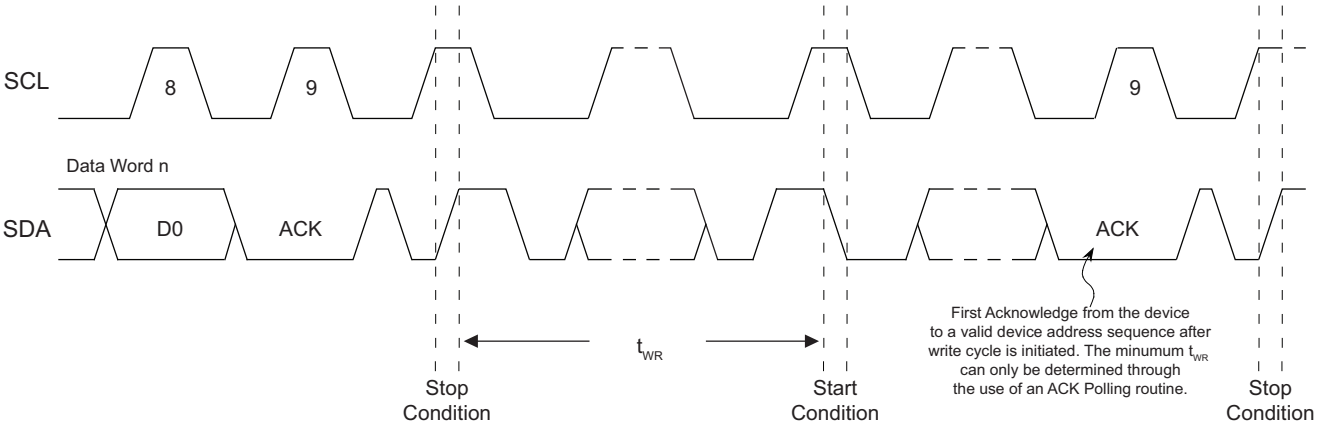
Figure 5-3. Acknowledge Polling Flow Chart



5.4 Write Cycle Timing

The length of the self-timed write cycle, or t_{WR}, is defined as the amount of time from the Stop condition that begins the internal Write operation, to the Start condition of the first Device Address byte sent to the AT24C04D that it subsequently responds to with an ACK. Figure 5-4 has been included to show this measurement. During the internally self-timed write cycle any attempts to read from or write to the memory array will not be processed.

Figure 5-4. Write Cycle Timing



5.5 Write Protection

The AT24C04D utilizes a hardware data protection scheme that allows the user to write protect the entire memory contents when the WP pin is at V_{CC} (or a valid V_{IH}). No write protection will be set if the WP pin is at GND or left floating.

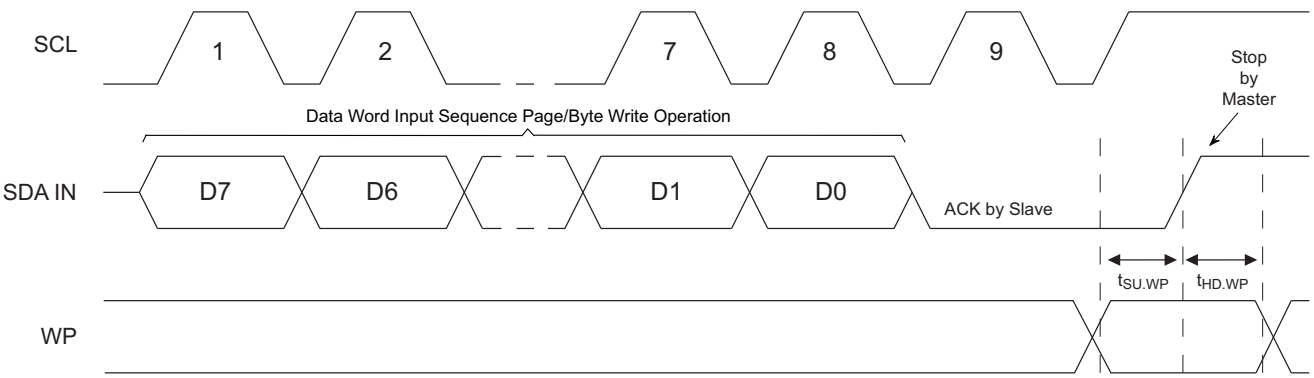
Table 5-1. AT24C04D Write Protect Behavior

WP Pin Voltage	Part of the Array Protected
V_{CC}	Full Array
GND	None — Write Protection Not Enabled

The status of the WP pin is sampled at the Stop condition for every Byte Write or Page Write command prior to the start of an internally self-timed Write operation. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle. The WP pin state must be valid with respect to the associated setup ($t_{SU.WP}$) and hold ($t_{HD.WP}$) timing as shown in the Figure 5-5 below. The WP setup time is the amount of time that the WP state must be stable before the Stop condition is issued. The WP hold time is the amount of time after the Stop condition that the WP state must remain stable.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the Device Address, Word Address, and Data bytes but no write cycle will occur when the Stop condition is issued, and the device will immediately be ready to accept a new Read or Write command.

Figure 5-5. Write Protect Setup and Hold Timing



6. Read Operations

Read operations are initiated the same way as Write operations with the exception that the Read/Write Select bit in the Device Address word must be a Logic 1. There are three Read operations:

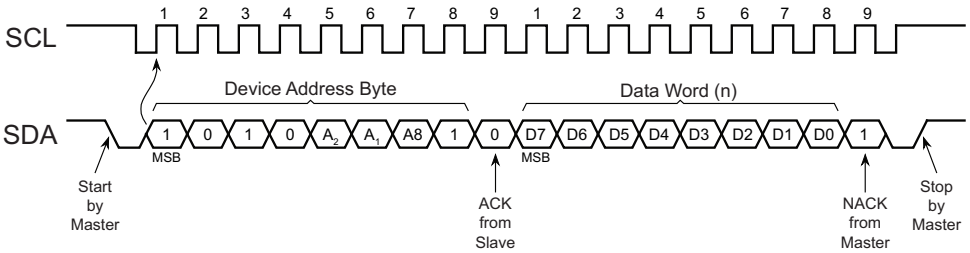
- Current Address Read
- Random Address Read
- Sequential Read

6.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V_{CC} is maintained to the part. The address “roll over” during read is from the last byte of the last page to the first byte of the first page of the memory.

A Current Address Read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid Device Address byte with the R/$\overline{W}$ bit set to Logic 1. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of Read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

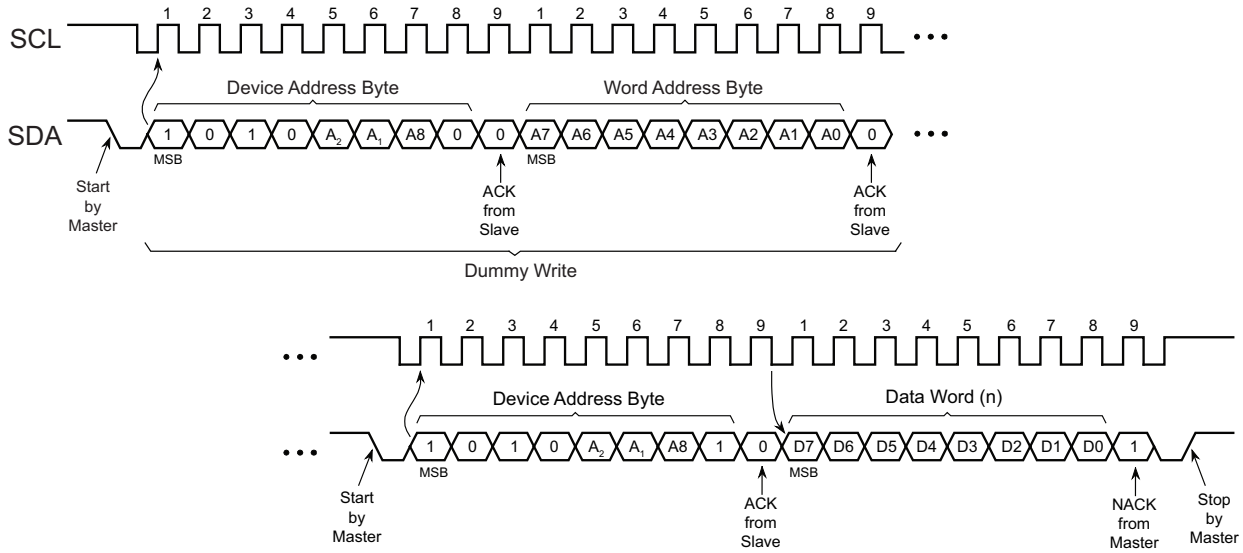
Figure 6-1. Current Address Read



6.2 Random Read

A Random Read begins in the same way as a Byte Write operation does to load in a new data word address. This is known as a “dummy write” sequence; however, the Stop condition of the Byte Write must be omitted to prevent the part from entering an internal write cycle. Once the Device Address and Word Address are clocked in and acknowledged by the EEPROM, the bus Master must generate another Start condition. The bus Master now initiates a Current Address Read by sending a Start condition, followed by a valid Device Address byte with the R/W bit set to Logic 1. The EEPROM will ACK the Device Address and serially clock out the data word on the SDA line. All types of Read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

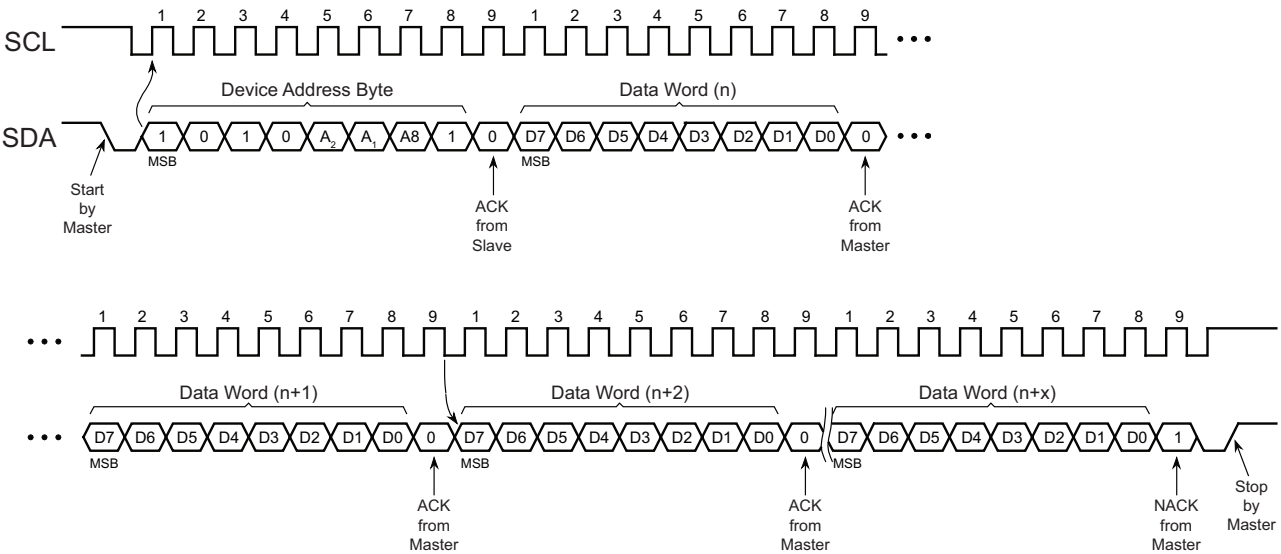
Figure 6-2. Random Read



6.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Read. After the bus Master receives a data word, it responds with an acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will “roll over” and the sequential read will continue from the beginning of the memory array. All types of Read operations will be terminated if the bus Master does not respond with an ACK (it NACKs) during the ninth clock cycle, which will force the device into standby mode. After the NACK response, the Master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 6-3. Sequential Read



7. Device Default Condition from Atmel

The AT24C04D is delivered with the EEPROM array set to Logic 1, resulting in FFh data in all locations.

8. Electrical Specifications

8.1 Absolute Maximum Ratings

Temperature under Bias . . . . . -55°C to +125°C

Storage Temperature . . . . . -65°C to +150°C

Supply Voltage
with respect to ground . . . . . -0.5V to +4.10V

Voltage on any pin
with respect to ground . . . . . -0.6V to V_{CC} + 0.5V

DC Output Current 5.0mA

Functional operation at the “Absolute Maximum Ratings” or any other conditions beyond those indicated in Section 8.2 “DC and AC Operating Range” is not implied or guaranteed. Stresses beyond those listed under “Absolute Maximum Ratings” and/or exposure to the “Absolute Maximum Ratings” for extended periods may affect device reliability and cause permanent damage to the device.

The voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot pulses that the device may be subjected to during the course of normal operation and does not imply or guarantee functional device operation at these levels for any extended period of time.

8.2 DC and AC Operating Range

Table 8-1. DC and AC Operating Range

		AT24C04D
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low Voltage Grade	1.7V to 3.6V

8.3 DC Characteristics

Table 8-2. DC Characteristics

Parameters are applicable over the operating range in specified Section 8.2, unless otherwise noted.

Symbol	Parameter	Test Conditions		Min	Typical[1]	Max	Units
V_{CC}	Supply Voltage			1.7		3.6	V
I_{CC1}	Supply Current, Read	V_{CC} = 1.8V[2]	Read at 400kHz		0.08	0.3	mA
		V_{CC} = 3.6V	Read at 1MHz		0.15	0.5	mA
I_{CC2}	Supply Current, Write	V_{CC} = 3.6V	Write at 1MHz		0.20	1.0	mA
I_{SB}	Standby Current	V_{CC} = 1.8V[2]	V_{IN} = V_{CC} or V_{SS}		0.08	0.4	µA
		V_{CC} = 3.6V			0.10	0.8	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[2]			-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[2]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V

Notes: 1. Typical values characterized at T_A = +25°C unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

8.4 AC Characteristics

Table 8-3. AC Characteristics

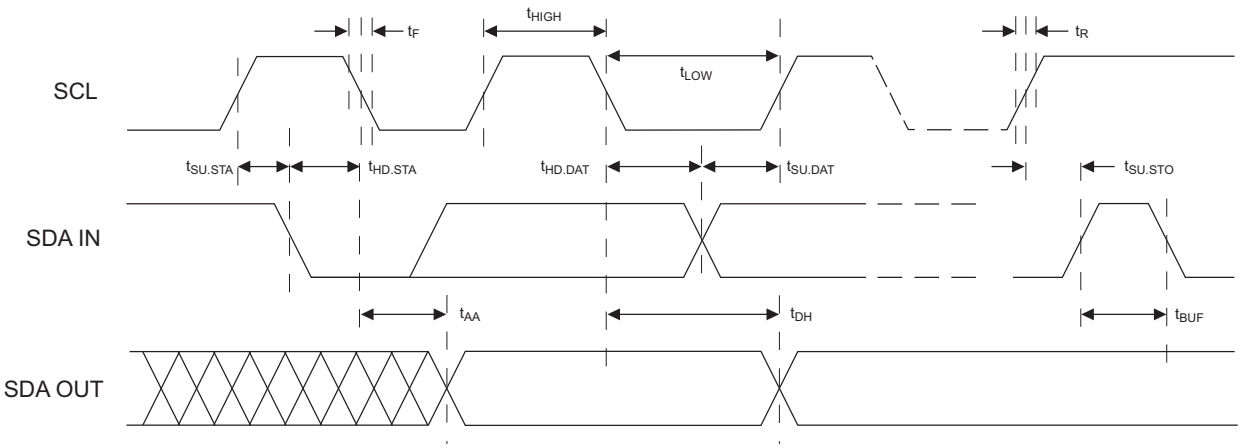
Parameters are applicable over operating range in Section 8.2 unless otherwise noted. Test conditions shown in Note 2.

Symbol	Parameter	Standard Mode V_{CC} = 1.7V to 3.6V		Fast Mode V_{CC} = 1.7V to 3.6V		Fast Mode Plus V_{CC} = 2.5V to 3.6V		Units
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	4,700		1,300		500		ns
t_{HIGH}	Clock Pulse Width High	4,000		600		400		ns
t_I	Input Filter Spike Suppression (SCL,SDA)(1)		100		100		100	ns
t_{AA}	Clock Low to Data Out Valid		4,500		900		450	ns
t_{BUF}	Bus Free Time between Stop and Start(1)	4,700		1,300		500		ns
$t_{HD.STA}$	Start Hold Time	4,000		600		250		ns
$t_{SU.STA}$	Start Set-up Time	4,700		600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	200		100		100		ns
t_R	Inputs Rise Time(1)		1,000		300		100	ns
t_F	Inputs Fall Time(1)		300		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	4,700		600		250		ns
$t_{SU.WP}$	Write Protect Setup Time	4,000		600		100		ns
$t_{HD.WP}$	Write Protect Hold Time	4,000		600		400		ns
t_{DH}	Data Out Hold Time	100		50		50		ns
t_{WR}	Write Cycle Time		5		5		5	ms

Notes: 1. These parameters are determined through product characterization and are not 100% tested in production.

2. AC measurement conditions:
   - C_L : 100pF
   - R_{PUP} (SDA bus line pull-up resistor to V_{CC}): 1.3kΩ (1000kHz), 4kΩ (400kHz), 10kΩ (100kHz)
   - Input pulse voltages: 0.3 x V_{CC} to 0.7 x V_{CC}
   - Input rise and fall times: ≤ 50ns
   - Input and output timing reference voltages: 0.5 x V_{CC}

Figure 8-1. Bus Timing



8.5 Power-Up Requirements and Reset Behavior

During a power-up sequence the V_{CC} supplied to the AT24C04D should monotonically rise from GND to the minimum V_{CC} level as specified in Section 8.2, with a slew rate no faster than 0.1V/µs.

8.5.1 Device Reset

To prevent inadvertent write operations or other spurious events from happening during a power-up sequence, the AT24C04D includes a power-on-reset (POR) circuit. Upon power-up, the device will not respond to any commands until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of reset and into standby mode.

The system designer must ensure that instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than the minimum V_{CC} level. Additionally, once the V_{CC} has surpassed the minimum V_{CC} level, the bus Master must wait at least t_{PUP} before sending the first command to the device. See Table 8-4 for the values associated with these power-up parameters.

Table 8-4. Power-up Conditions[1]

Symbol	Parameter	Min	Max	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept commands.	100		µs
V_{POR}	Power-On Reset Threshold Voltage.		1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles.	1		ms

Note: 1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT24C04D drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the V_{CC} pin to GND, waiting at least the minimum t_{POFF} time, and then performing a new power-up sequence in compliance with the requirements defined in this section.

8.6 Pin Capacitance

Figure 8-2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 3.6V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_1, A_2, SCL)	6	pF	V_{IN} = 0V

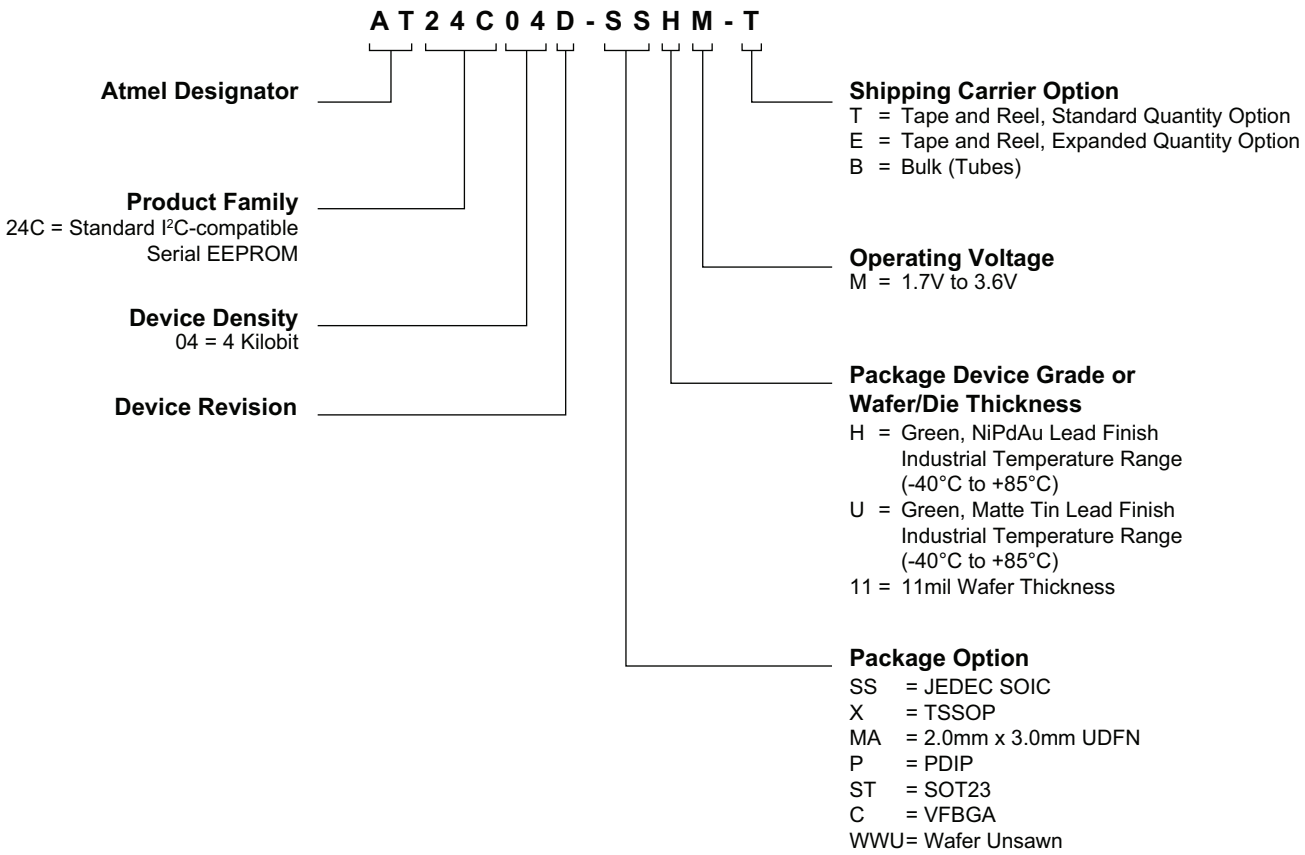
Note: 1. This parameter is characterized but is not 100% tested in production.

8.7 EEPROM Cell Performance Characteristics

Operation	Test Condition	Min	Max	Units
Write Endurance[1]	T_A = 25°C, V_{CC} (min) < V_{CC} < V_{CC} (max) Byte or Page Write Mode	1,000,000	—	Write Cycles
Data Retention[2]	T_A = 55°C, V_{CC} (min) < V_{CC} < V_{CC} (max)	100	—	Years

Notes: 1. Write endurance performance is determined through characterization and the qualification process.
2. The data retention capability is determined through qualification and is checked on each device in production.

9. Ordering Code Detail



10. Ordering Information

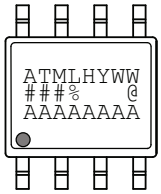
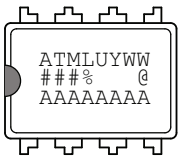
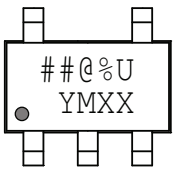
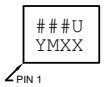
Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT24C04D-SSHM-T	NiPdAu (Lead-free/Halogen-free)	8S1	Tape and Reel	4,000 per Reel	Industrial Temperature (-40°C to 85°C)
AT24C04D-SSHM-B			Bulk (Tubes)	100 per Tube	
AT24C04D-XHM-T		8X	Tape and Reel	5,000 per Reel	
AT24C04D-XHM-B			Bulk (Tubes)	100 per Tube	
AT24C04D-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C04D-MAHM-E			Tape and Reel	15,000 per Reel	
AT24C04D-PUM	Matte Tin (Lead-free/Halogen-free)	8P3	Bulk (Tubes)	50 per Tube	
AT24C04D-STUM-T		5TS1	Tape and Reel	5,000 per Reel	
AT24C04D-CUM-T	SnAgCu Ball (Lead-free/Halogen-free)	8U3-1	Tape and Reel	5,000 per Reel	
AT24C04D-WWU11M(1)	N/A	Wafer Sale	Note 1		

Note: 1. For wafer sales, please contact Atmel Sales.

Package Type	
8S1	8-lead, 0.150” wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.0mm x 3.0mm x 0.6mm body, 0.5mm Pitch, Ultra Thin Dual Flat No Lead (UDFN)
8P3	8-lead, 0.300" wide, Plastic Dual In-line Package (PDIP)
5TS1	5-lead, 1.60mm body, Plastic Thin Shrink Small Outline (SOT23)
8U3-1	8-ball, 1.5mm x 2.0mm body, 0.5mm pitch, Very thin Fine Ball Grid Array (VFBGA)

11. Part Markings

AT24C04D: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-pad UDFN
		2.0 x 3.0 mm Body 
8-lead PDIP	**5-lead SOT-23**	**8-ball VFBGA**
		1.5 x 2.0 mm Body 

Note 1: ● designates pin 1
Note 2: Package drawings are not to scale
Note 3: For SOT23 package with date codes before 7B, the bottom line (YMXX) is marked on the bottom side and there is no Country of Assembly (@) mark on the top line.

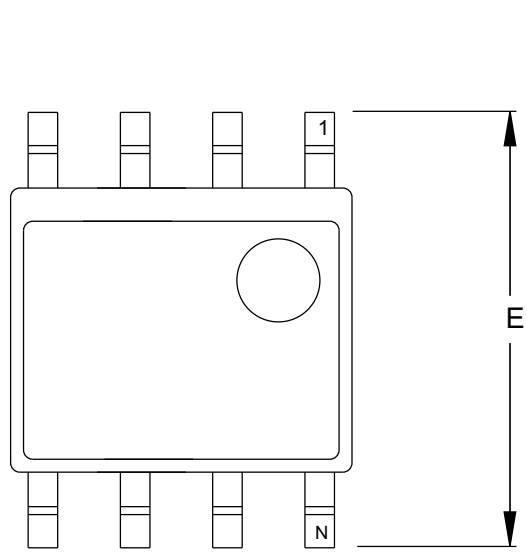
Catalog Number Truncation			
AT24C04D		Truncation Code ###: 04D / ##: 4D	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
6: 2016 8: 2020 7: 2017 9: 2021 6: 2018 0: 2023 9: 2019 1: 2024	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu U: Industrial/Matte Tin/SnAgCu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

12/6/16

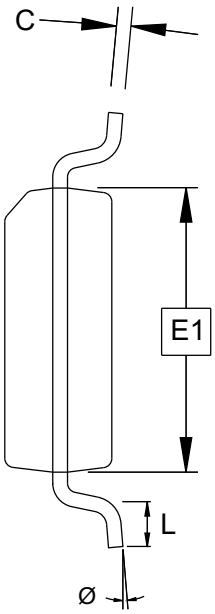
Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **24C04DSM**, AT24C04D Package Marking Information	**DRAWING NO.** 24C04DSM	**REV.** B

12. Packaging Information

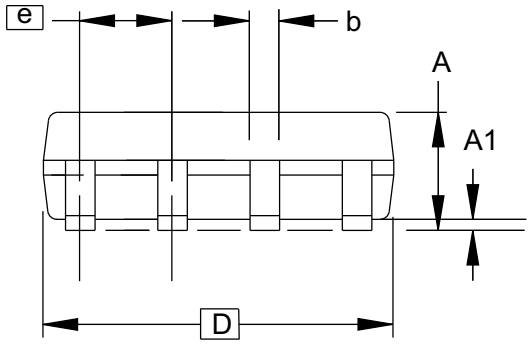
12.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

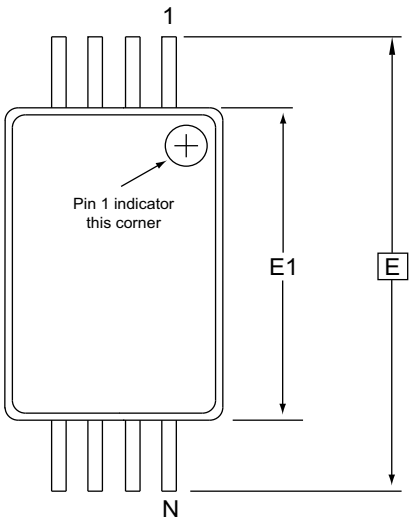
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

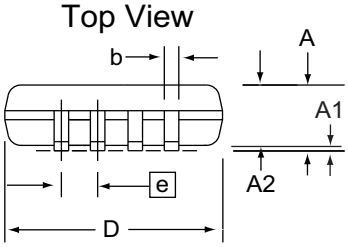
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

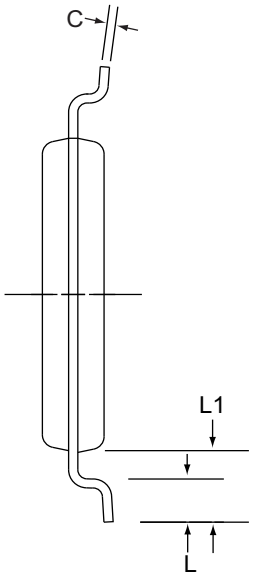
12.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

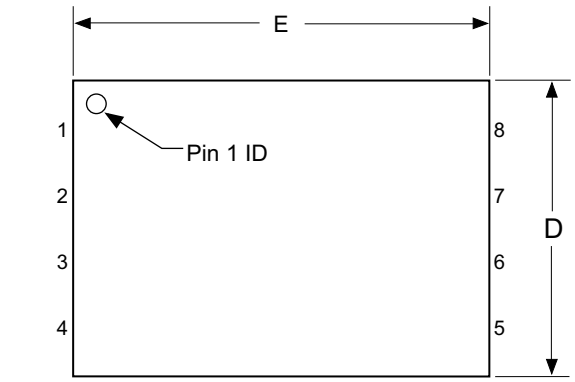
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

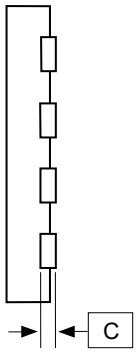
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

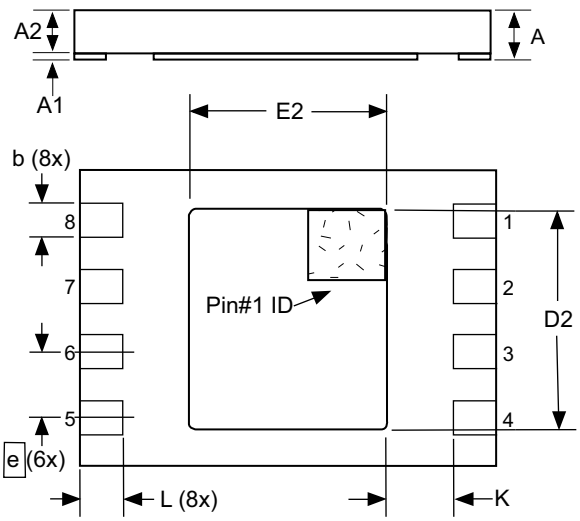
12.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

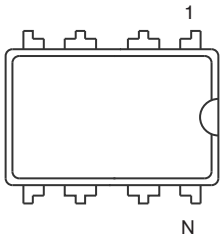
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

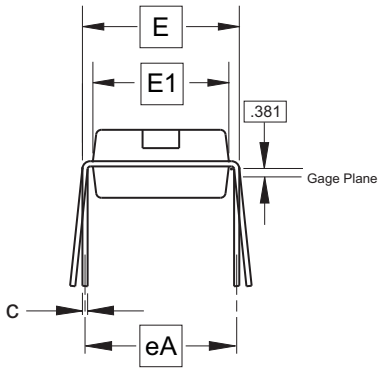
11/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** G

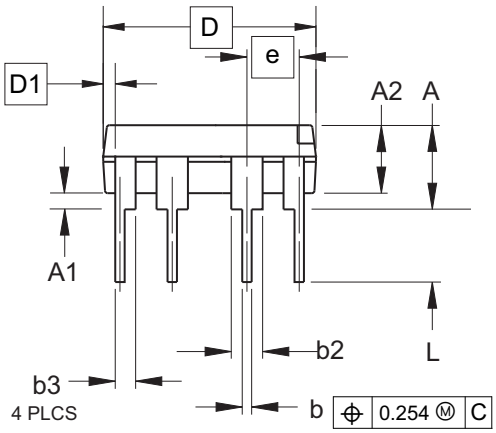
12.4 8P3 — 8-lead PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

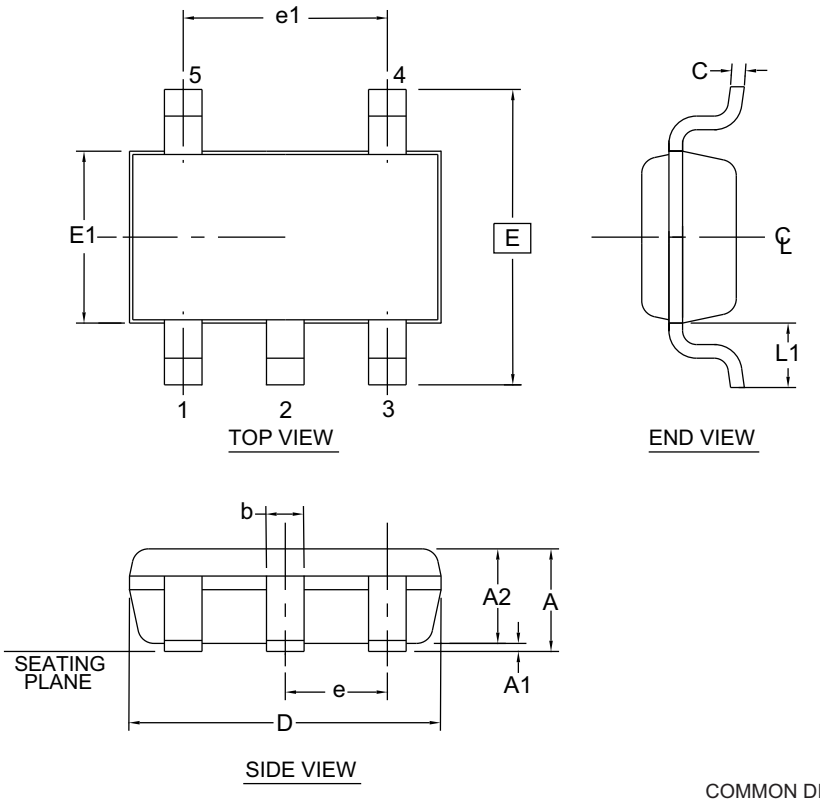
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
c	0.203	0.254	0.356	
D	9.017	9.271	10.160	3
D1	0.127	0.000	0.000	3
E	7.620	7.874	8.255	4
E1	6.096	6.350	7.112	3
e	2.540 BSC			
eA	7.620 BSC			4
L	2.921	3.302	3.810	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

07/31/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP)	GPC PTC	DRAWING NO. 8P3	REV. E

12.5 5TS1 — 5-lead SOT23



1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

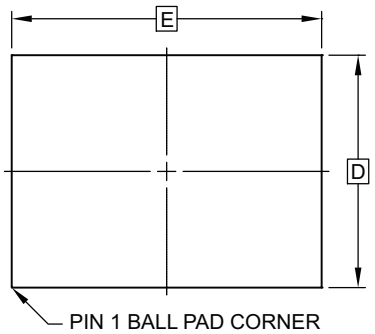
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.00	
A1	0.00	-	0.10	
A2	0.70	0.90	1.00	
c	0.08	-	0.20	3
D	2.90 BSC			1,2
E	2.80 BSC			1,2
E1	1.60 BSC			1,2
L1	0.60 REF			
e	0.95 BSC			
e1	1.90 BSC			
b	0.30	-	0.50	3,4

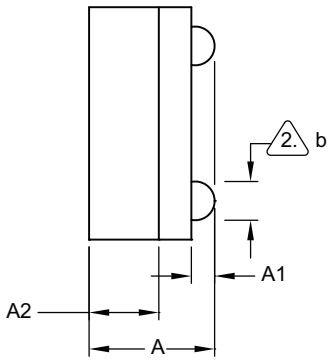
5/31/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 5TS1, 5-lead 1.60mm Body, Plastic Thin Shrink Small Outline Package (Shrink SOT)	GPC TSZ	DRAWING NO. 5TS1	REV. D

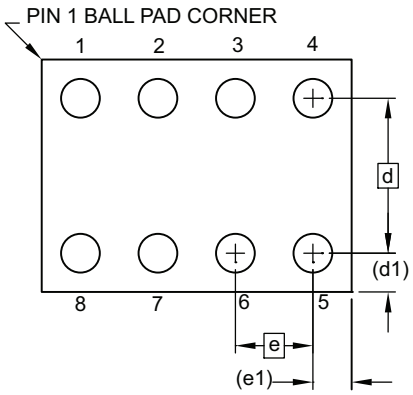
12.6 8U3-1 — 8-ball VFBGA



TOP VIEW



SIDE VIEW



BOTTOM VIEW
8 SOLDER BALLS

Notes:

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter.
3. Solder ball composition shall be 95.5Sn-4.0Ag-.5Cu.

COMMON DIMENSIONS
(Unit of Measure - mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.73	0.79	0.85	
A1	0.09	0.14	0.19	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.0 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/11/13

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8U3-1, 8-ball, 1.50mm x 2.00mm body, 0.50mm pitch, Very Thin, Fine-Pitch Ball Grid Array Package (VFBGA)	GPC GXU	DRAWING NO. 8U3-1	REV. F

13. Revision History

Doc. No.	Date	Comments
8896E	01/2017	Updated Power On Requirements and Reset Behavior section
8896D	12/2016	Part marking SOT23: - Moved backside mark (YMXX) to front side line2. - Added @ = Country of Assembly.
8896C	01/2015	Added the 100kHz timing set for reference, the UDFN extended quantity option, and the figure for “System Configuration Using 2-Wire Serial EEPROMs”. Updated the 8MA2 and 8P3 package outline drawings.
8896B	07/2014	Updated from preliminary to complete status and the 8X and 8MA2 package drawings.
8896A	03/2014	Initial document release.

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