Hermetic, Multi-Chip Module (MCM)

32Mb, 1M x 32, 3.3Volt Boot Block FLASH Array

Available via Applicable Specifications:

- MIL-PRF-38534, Class H
- DSCC SMD 5962-09205

FEATURES

- 32Mb device, total density, organized as 1M x 32
- Bottom Boot Block (Sector) Architecture
- Operation with single 3.3V Supply
- Available in multiple Access time variations
- Individual byte control via individual byte selects (CSx\)
- Low Power CMOS
- 20 years data retention
- 1,000,000 Program/Erase Cycles per sector minimum
- Sector Architecture:
  - One 16K byte, two 8K byte, one 32K byte and fifteen 64Kbyte sectors
- Any combination of sectors can be concurrently erased
- MCM supports full array (multi-chip) Erase
- Embedded Erase and Program Algorithms
- Erase Suspend/Resume; Supports reading data from or programming data to a sector not being Erased
- TTL Compatible Inputs and Outputs
- Military and Industrial operating temperature ranges

OPTION — MARKING

Access Speed

70ns*	-70
90ns	-90
100ns	-100
120ns	-120

*Contact factory

Package

Ceramic Quad Flat Pack	Q
Ceramic Hex Inline Pack	P

Temperature Range

Full Mil (MIL-PRF-38534, Class H)	/Q
Military Temp (-55°C to +125°C)	/XT
Industrial (-40°C to +85°C)	/IT

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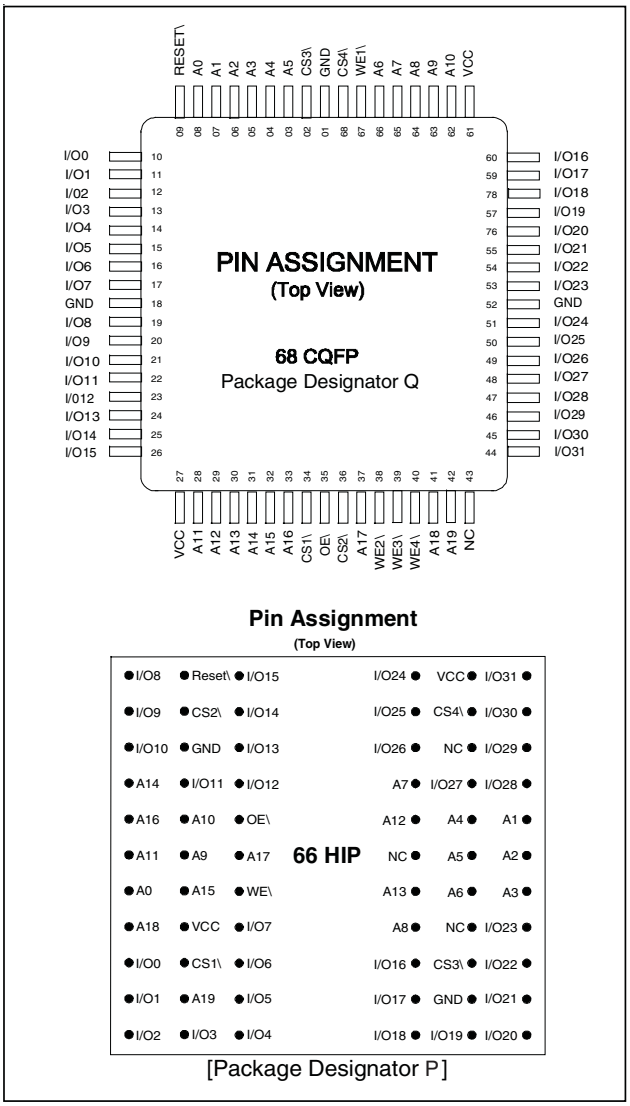
FIGURE 1: PIN ASSIGNMENT
(Top View)



GENERAL DESCRIPTION

The AS8FLC1M32B is a 32Mb FLASH Multi Chip Module organized as 1M x 32 bits. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology. The military grade product is manufactured in compliance to the MIL-PRF-38534 specifications, making the AS8FLC1M32B ideally suited for military or space applications. The module is offered in a 68-lead 0.990 inch square ceramic quad flat pack or 66-lead 1.185inch square ceramic Hex In-line Package (HIP). The CQFP package design is targeted for those applications, which require low profile SMT Packaging.

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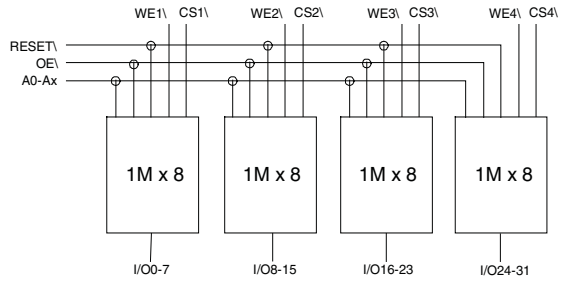
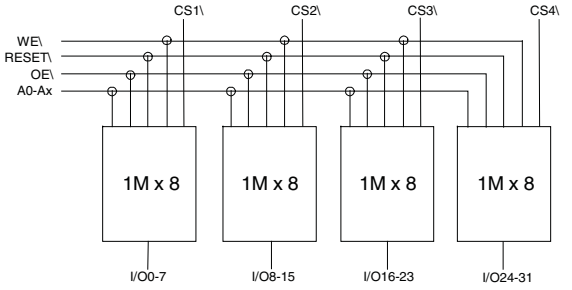
BLOCK DIAGRAM

68-Ld. CQFP, Package " Q "



BLOCK DIAGRAM

66-Ld. HIP, Package "P"



The device requires only a single 3.3volt power supply for both READ and WRITE operations. Internally generated and regulated voltages are provided for the program and erase functions.

The device is entirely command set compatible with the JEDEC SINGLE POWER FASH STANDARD. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for the programming or erase function(s). Reading data out of the array is similar to reading from other electrically programmable devices.

Device programming occurs by executing the program command sequence. This initiates the EMBEDDED PROGRAM algorithm that automatically times the WRITE PULSE widths and cycle and verifies each cell for proper cell margins. The UNLOCK BYPASS mode facilitates faster programming times by requiring only two WRITE cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm, an internal algorithm that automatically pre-programs the array before executing the erase operation. During erasure, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data\ Polling) and DQ6 (toggle) STATUS BITS. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

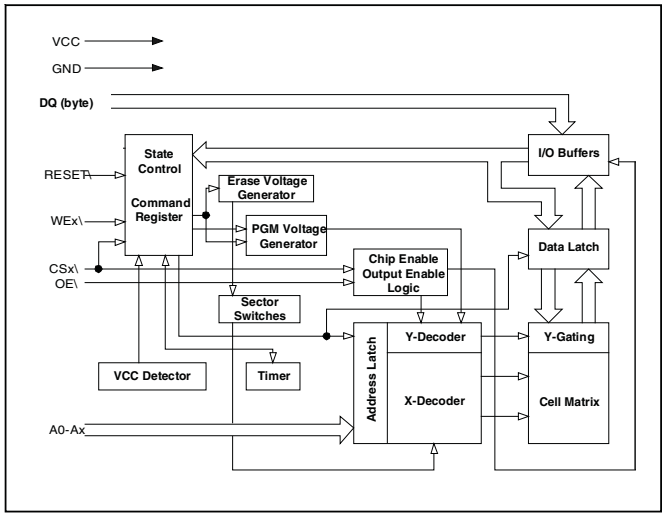
The SECTOR ERASE ARCHITECTURE allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from Micross.

Hardware data protection measures include a low VCC detector that automatically inhibits WRITE operations during power transitions. The hardware sector protection features disables both program and erase operation in any combination of the sectors of memory. This can be achieved in-system or via specially adapted commercial programming equipment.

The ERASE SUSPEND feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector which is not selected for erasure. True BACKGROUND ERASE can thus be achieved.

The HARDWARE RESET\ PIN terminates any operation in progress and resets the internal state machine to a READ operation. The RESET\ pin may be tied to the system reset circuitry.

LOGIC DIAGRAM (Byte)



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A system reset would then also reset the FLASH device, enabling the system microprocessor to read the boot-up firmware from the FLASH memory array. The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the AUTOMATIC SLEEP MODE. The system can also place the device into the STANDBY mode. Power consumption is greatly reduced in both these modes.

Device Bus Operations

This section describes the use of the command register for setting and controlling the bus operations. The command register itself does not occupy any addressable memory locations. The register is composed of a series of latches that store the commands, addresses and data information needed to execute the indicated command. The contents of the register serve as the input to the internal state machine. The state machine output dictates the function of the device. Table 1 lists the device bus operations, the inputs and control/stimulus levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CSx\ and OE\ pins to VIL. Chip Select CSx\ is the power and chip select control of the byte or bytes targeted by the system (user). Output Enable [OE\] is the output control and gates array data to the output pins. Write (byte) Enables [WEx\] should remain at VIH levels.

The internal state machine is set for reading array data upon device power-up, or after a HARDWARE RESET. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid data on the device address inputs produce valid data on the data outputs. The device remains enabled for read access until the command register contents are altered.

See READING ARRAY DATA for more information. Refer to AC Read Operations table data for timing specifications relevant to this operational mode.

Writing Commands/Command Sequences

To WRITE a command or command sequence, the system must drive CSx\, WEx\ to VIL and OE\ to VIH.

An ERASE command operation can erase one sector, multiple sectors, or the entire array. Table 2 indicates the address space contained within each sector within the array. A sector address
consists of the address bits required to uniquely select a sector.
The “Command Definitions” section has details on erasure of a single, multiple sectors, the entire array or suspending/ resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on each of the Data input/output bits within each byte of the MCM FLASH array. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

ICC2 in the DC Characteristics table represents that active current specification for the WRITE mode. The AC Characteristics section contains timing specifications for Write Operations.

Table 1

RESET\	CS1\	CS2\	CS3\	CS4\	WE1\	WE2\	WE3\	WE4\	OE\	Operation	Addresses	Data Bus [DQ0-DQx]
H	L	H	H	H	H	H	H	H	L	READ	A0-Ax In	D0-D7 Out
	H	L	H	H								D8-D15 Out
	H	H	L	H								D16-D23 Out
	H	H	H	L								D24-D31 Out
	L	L	L	L								D0-D31 Out
H	L	H	H	H	L	H	H	H	H	WRITE	A0-Ax In	D0-D7 In
	H	L	H	H	H	L	H	H				D8-D15 In
	H	H	L	H	H	H	L	H				D16-D23 In
	H	H	H	L	H	H	H	L				D24-D31 In
	L	L	L	L	L	L	L	L				D0-D31 In
VCC+/-0.3V	VCC+/-0.3V	VCC+/-0.3V	VCC+/-0.3V	VCC+/-0.3V	X	X	X	X	X	Standby	X	
X	L	L	L	L	H	H	H	H	H	Output Disable	X	
L	X	X	X	X	X	X	X	X	X	Reset	X	
VID	L	L	L	L	L	L	L	L	H	Sector Protect	Sector Address, A6=L, A1=H, A0=L	D-In, D-Out
VID	L	L	L	L	L	L	L	L	H	Sector Un-Protect	Sector Address, A6=H, A1=H, A0=L	D-In, D-Out
VID	X	X	X	X	X	X	X	X	X	Temporary Sector Un-Protect	A-In	D-In
Legend	L= Logic Low=VIL, H= Logic High=VIH, VID= 12.0+/-0.5V, X= Don't Care, Ain=Address In, Dout=Data Out											
Notes (*)												

Table 2

Sector	A19	A18	A17	A16	A15	A14	A13	Sector Size (Kbytes)
SA0	0	0	0	0	0	0	X	16
SA1	0	0	0	0	0	1	0	8
SA2	0	0	0	0	0	1	1	8
SA3	0	0	0	0	1	X	X	32
SA4	0	0	0	1	X	X	X	64
SA5	0	0	1	0	X	X	X	64
SA6	0	0	1	1	X	X	X	64
SA7	0	1	0	0	X	X	X	64
SA8	0	1	0	1	X	X	X	64
SA9	0	1	1	0	X	X	X	64
SA10	0	1	1	1	X	X	X	64
SA11	1	0	0	0	X	X	X	64
SA12	1	0	0	1	X	X	X	64
SA13	1	0	1	0	X	X	X	64
SA14	1	0	1	1	X	X	X	64
SA15	1	1	0	0	X	X	X	64
SA16	1	1	0	1	X	X	X	64
SA17	1	1	1	0	X	X	X	64
SA18	1	1	1	1	X	X	X	64

Program and Erase Operation Status

During an ERASE or PROGRAM operation, the system may check the status of the operation by reading the status bits on each of the seven data I/O bits within each byte of the MCM FLASH array. Standard READ cycle timings and ICC read specifications apply. Refer to "Write Operation Status" for more information, and to "AC Characteristics" for timing specifications.

Standby Mode

When the system is not READING or WRITING to the device, it can place the device in the standby mode to save on power consumption.

The device enters the CMOS STANDBY mode when the CSx\ and RESET\ pins are held at VCC+/-0.3v. If CSx\ and RESET\ are held at VIH, but not within VCC+/-0.3v, the device will be in STANDBY mode but at levels higher than achievable in full CMOS STANDBY. The device requires standard access time (tCE) for read access when the device is in either of these STANDBY modes, before it is ready to READ data.

If the device is deselected during ERASURE or PROGRAMMING, the device draws active current until the operation is completed.

In the DC Characteristics table, ICC3 and ICC4 represent the STANDBY MODE currents.

Automatic Sleep Mode

The AUTOMATIC SLEEP mode minimizes FLASH device energy consumption. The device automatically enables this mode when addresses remain stable for tACC + 30ns.

The AUTOMATIC SLEEP mode is independent of the CSx\, WEx\ and OE\ control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC5 in the "DC Characteristics Table represents the AUTOMATIC SLEEP mode current usage.

RESET\: Hardware Reset Pin

The RESET\ pin provides a hardware method of resetting the device to reading array data. When the RESET\ pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all READ/WRITE commands for the duration of the RESET\ pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET\ pulse. When RESET\ is held at VSS+/-0.3v, the device draws CMOS STANDBY current (ICC4). If RESET\ is held at VIL but not within the limits of VCC +/- 0.3v, the MCM Array will be in STANDBY, but current limits will be higher than those listed under ICC4.

The RESET\ pin may be tied to the system reset circuitry. A system reset would thus also reset the FLASH array, enabling the system to read the boot-up firmware code from the boot block area of the memory.

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Autoselect Code Table

PROGRAM or ERASE operation is not executing, the RESET operation is completed within a time of tREADY. The system can read data tRH after the RESET\ pin returns to VIH.

Refer to the "AC Characteristics" tables for RESET\ parameters.

Output Disable Mode

When the OE\ input is at VIH, output from the device is disabled. The output pins are placed in the high Impedance State.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification through identifier codes output via the appropriate Byte DQ's. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

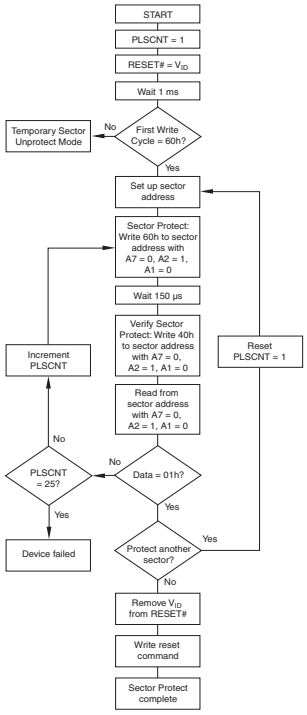
When using programming equipment (modified to support multi-byte devices, or supplied from the programming equipment provider as such), the autoselect mode requires VID (11.5v to

Bottom Boot Sector Address Table

12.5v) on address pin A9. Address pins A6, A1, and A0 must be as shown in the Autoselect Table below. In addtion, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on the appropriate Byte DQ's.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register.

Sector Protect Algorithm Flow



Description	CS1\	CS2\	CS3\	CS4\	OEX\	WEx\	A19 to A13	A12 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQx [Output]
Manufacturers ID	L	H	H	H	L	H	X	X	VID	X	L	X	L	L	DQ0-7 [01h]
	X	L	H	H	L	H	X	X	VID	X	L	X	L	L	DQ8-15 [01h]
	H	H	L	H	L	H	X	X	VID	X	L	X	L	L	DQ16-23 [01h]
	H	H	H	L	L	H	X	X	VID	X	L	X	L	L	DQ24-31 [01h]
Device ID	L	H	H	H	L	H	X	X	VID	X	L	X	L	H	DQ0-7 [5Bh]
	H	L	H	H	L	H	X	X	VID	X	L	X	L	H	DQ8-15 [5Bh]
	H	H	L	H	L	H	X	X	VID	X	L	X	L	H	DQ16-23 [5Bh]
	H	H	H	L	L	H	X	X	VID	X	L	X	L	H	DQ24-31 [5Bh]
Sector Protection Verification	L	H	H	H	L	H	SA	X	VID	X	L	X	H	L	DQ0-7 [01h] Protected
	H	L	H	H	L	H	SA	X	VID	X	L	X	H	L	DQ8-15 [01h] Protected
	H	H	L	H	L	H	SA	X	VID	X	L	X	H	L	DQ16-23 [01h] Protected
	H	H	H	L	L	H	SA	X	VID	X	L	X	H	L	DQ24-31 [01h] Protected
	L	H	H	H	L	H	SA	X	VID	X	L	X	H	L	DQ0-7 [00h] Un-Protected
	H	L	H	H	L	H	SA	X	VID	X	L	X	H	L	DQ8-15 [00h] Un- Protected
	H	H	L	H	L	H	SA	X	VID	X	L	X	H	L	DQ16-23 [00h]Un-Protected
	H	H	H	L	L	H	SA	X	VID	X	L	X	H	L	DQ24-31 [00h] Un-Protected

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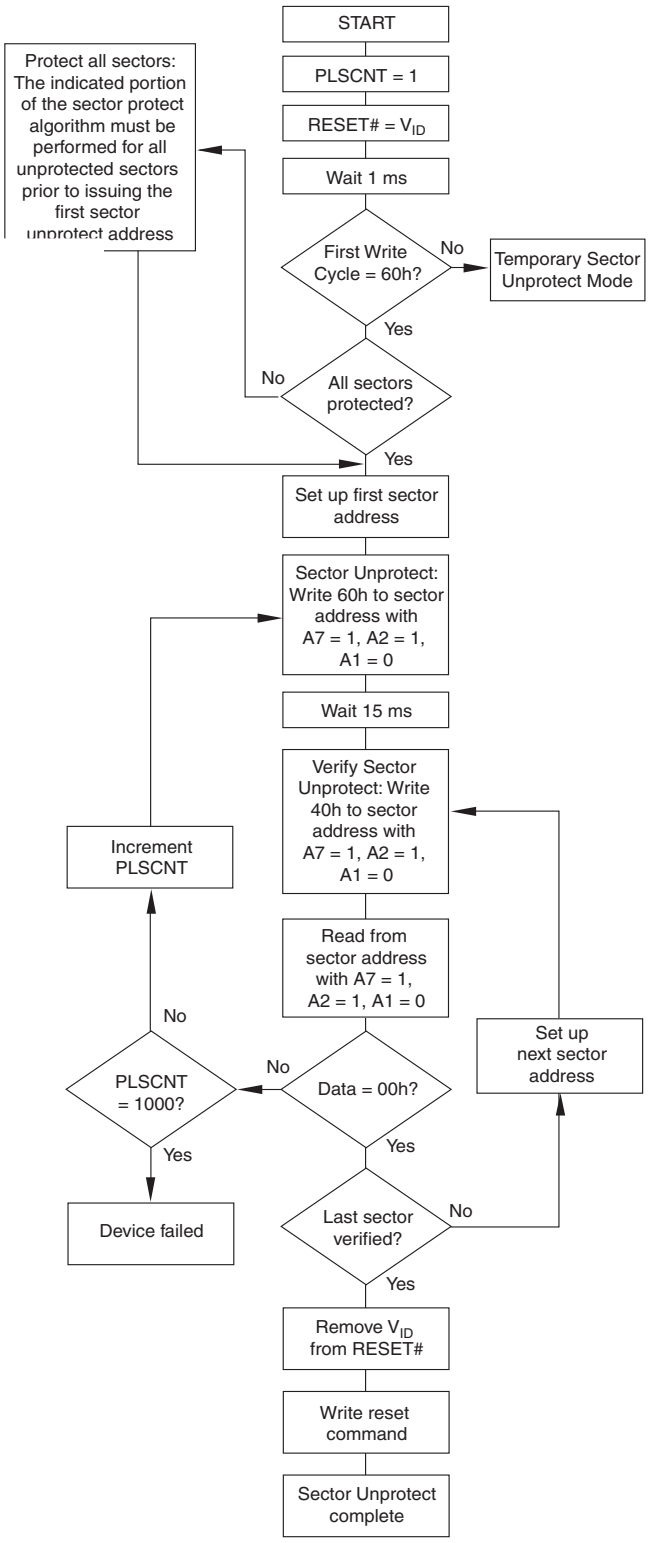
Sector Un-Protect Algorithm Flow



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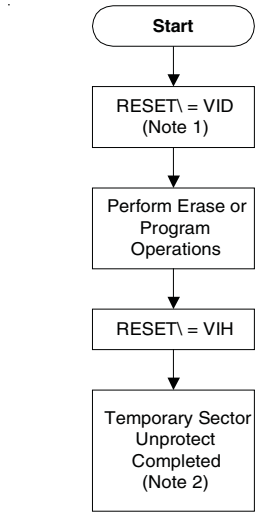
Temporary Sector Unprotect

This feature allows temporary un-protection of previously protected sectors to change data in-system. Setting the RESET\ pin to VID activates the sector Unprotect mode. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once VID is removed from the RESET\ pin, all the previously protected sectors are protected again. The diagram below depicts the algorithm flow for this operation.

Temporary Sector Unprotect Diagram



NOTES:
1. All protected sectors unprotected
2. All previously protected sectors are protected once again

Hardware Data Protection

The command sequence requirements of UNLOCK cycles for PROGRAMMING or ERASING provides data protection against inadvertent WRITES. In addition, the following hardware data protection measures prevent accidental ERASURE or PROGRAMMING, which might otherwise be caused by spurious system level signals during VCC power-up and power-down transitions, or from system noise.

Low VCC WRITE Inhibit

When VCC is less than VLKO, the device does not accept any WRITE cycles. This protects data during VCC power-up and power-down. The system must provide the proper signals to the control pins to prevent unintentional WRITES when VCC is greater than VLKO.

Write Pulse "GLITCH" Protection

Noise pulses of less than 5ns (typical) on OE\, CSx\ or WEx\ do not initiate a WRITE cycle.

Logical Inhibit

WRITE cycles are inhibited by holding any one of OE\=VIL, CSx\=VIH or WEx\=VIH. To initiate a WRITE cycle, CSx\ and WEx\ must be a logical zero while OE\ is a logical one.

Power-Up WRITE Inhibit

If WEx\=CSx\=VIL and OE\=VIH during power-up, the device does not accept commands on the rising edge of WEx\. The internal state machine is automatically reset to READING array data on power-up.

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. The COMMAND REGISTER TABLE defines the valid register command sequences for this device Module. WRITING incorrect address and data values or WRITING them in the improper sequence resets the device to READING array data.

All addresses are latched on the falling edge of WEx\ or CSx\, whichever happens later. All data is latched on the rising edge of WEx\ or CSx\, whichever happens first. Refer to the AC timing references for correct timings of the appropriate signals.

Reading Array Data

The device is automatically set to READING Array data after device power-up. No commands are required to retrieve data. The device is also ready to READ data after completing an Embedded Program or Embedded Erase operation.

After the device accepts an ERASE Suspend command, the device enters the ERASE Suspend Mode. The system can read array data using the standard READ timings, except that if it READS at an address within Erase-Suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend Mode, the system may once again READ array data with the same exception.

The system must issue the reset command to re-enable the device for reading array data if DQ5, DQ13, DQ21 and DQ29 goes high, or while in the autoselect mode.

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Reset Command

WRITING the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The RESET command may be WRITTEN between the sequence cycles in an ERASE command sequence before ERASING begins. This resets the device to READING array data. Once ERASURE begins, the device ignores RESET command requests until the first initiation of the operation has completed.

The RESET command may be WRITTEN between the sequence cycles in a program command sequence and before programming begins. This RESETS the device to READING Array data. Once programming begins, the device ignores additional RESET command requests until the current operation has completed.

The RESET command may be written between the sequence cycles in an Autoselect command sequence. Once in the Autoselect Mode, the reset command must be WRITTEN to return to READING Array data.

Autoselect Command Sequence

The Autoselect command sequence allows the host system to access the manufacturer and device codes, allowing the user determination as to whether or not a Sector is protected. This method is an alternative to DEVICE PROGRAMMERS but requires VID on Address bit 9 (A9).

The Autoselect command sequence is initiated by WRITING two UNLOCK cycles, followed by the AUTOSELECT COMMAMD. The device then enters the AUTOSELECT mode, and the system may read at any address, any number of times, without initiating another command.

A READ cycle at Address XX00h retrieves the manufacturer code. A READ cycle at Address XX01h returns the device code. A READ cycle containing a Sector Address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is un-protected.

Byte Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock WRITE cycles, followed by the PROGRAM set-up command. The program address and data are WRITTEN next, which in turn initiates the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated PROGRAM pulses and verifies the programmed cell margin.

When the Embedded Program algorithm is complete, the device then returns to READING array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ31, DQ30, DQ23, DQ22, DQ15. DQ14, DQ7, DQ6.

Any commands WRITTEN to the device during the Embedded Program algorithm are ignored. Note that a HARDWARE RESET immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to READING Array data, to ensure data integrity.

PROGRAMMING is allowed in any sequence and across Sector Boundaries. A bit cannot be PROGRAMMED from a "0" back to a "1", this can only be accomplished via an ERASE operation.

Unlock Bypass Command Sequence

The UNLOCK BYPASS feature allows the system to program bytes to the device faster than using the standard program command sequence. The UNLOCK BYPASS command sequence is initiated by first WRITING two UNLOCK cycles. This is followed by a third WRITE cycle containing the UNLOCK BYPASS command, 20h. The device then enters the UNLOCK BYPASS mode. A two-cycle UNLOCK BYPASS command operation is all that is required to PROGRAM in this mode. The first cycle in this sequence contains the UNLOCK BYPASS program command, A0h; the second cycle contains the program address and data. Additional data is PROGRAMMED in the same manner. This mode dispenses with the initial two UNLOCK cycles required in the standard PROGRAM command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care fore both cycles. The device then returns to READING Array data.

Chip Erase Command Sequence

CHIP ERASE is a six-bus cycle operation. The CHIP ERASE command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional UNLOCK WRITE cycles are then followed by the chip ERASE command, which in turn invokes the Embedded ERASE algorithm. The device does not require the system to PRE-PROGRAM prior to ERASE. The Embedded ERASE algorithm automatically PRE-PROGRAMS and VERIFIES the entire Array for an all Zero data pattern prior to electrical ERASE. The system is not required to provide any controls or timing during these operations.
Any commands WRITTEN to the chip during the Embedded ERASE operation are ignored. Note that a HARDWARE RESET

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Any commands WRITTEN to the chip during the Embedded ERASE operation are ignored. Note that a HARDWARE RESET during the chip erase operation immediately terminates the operation. The CHIP ERASE command sequence should be reinitiated once the device has returned to READING Array data, to ensure data integrity.

The system can determine the status of the erase operation by using byte data from each of the four bytes. When the Embedded ERASE Algorithm is complete, the device returns to READING Array data and Addresses are no longer latched.

Sector Erase Command Sequence

SECTOR ERASE is a six-bus cycle operation. The SECTOR ERASE command sequence is initiated by WRITING two UNLOCK cycles, followed by a SET-UP command. Two additional UNLOCK WRITE cycles are then followed by the address of the sector to be ERASED, and the SECTOR ERASE command.

The device does not require the system to PREPROGRAM the memory prior to ERASE. The Embedded ERASE Algorithm automatically PROGRAMS and verifies the sector for an all zero data pattern prior to electrical ERASE. The system is not required to provide any controls or timings during these operations.

After the command sequence is WRITTEN, a SECTOR ERASE time-out of 50uS begins. During the time-out period, additional Sector Addresses and SECTOR ERASE commands may be WRITTEN. Loading the SECTOR ERASE buffer may be done in any sequence and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50uS, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last SECTOR ERASE command is WRITTEN. If the time between additional SECTOR ERASE commands can be assumed to be less than 50uS, the system need not monitor DQ3, DQ11, DQ19 or DQ27 to determine if the SECTOR ERASE has timed out. The time-out begins from the rising edge of the final WEx\ pulse in the command sequence.

Once the SECTOR ERASE operation has begun, only the ERASE SUSPEND command is valid. All other commands are ignored. Note that a HARDWARE RESET during the SECTOR ERASE operation immediately terminates the operation. The SECTOR ERASE command sequence should be reinitiated once

When the Embedded Erase Algorithm is complete, the device returns to READING Array data and addresses are no longer latched. The system can determine the status of the ERASE operation by using DQ2, DQ6, and DQ7 of Byte 1; DQ10, DQ14 and DQ15 of Byte 2; DQ18, DQ22 and DQ23 of Byte 3 as well as DQ26, DQ30 and DQ31 of Byte 4.

Erase Suspend/Erase Resume Commands

The ERASE SUSPEND command allows the system to interrupt a SECTOR ERASE operation and then READ data from, or PROGRAM data to, any sector not selected for ERASURE. This command is valid only during the SECTOR ERASE command sequence. The ERASE SUSPEND command is ignored if WRITTEN during the CHIP ERASE operation or Embedded Program algorithm. WRITING the ERASE SUSPEND command during the SECTOR ERASE time-out immediately terminates the time-out period and SUSPENDS the ERASE operation. Addresses are “don’t-cares” when WRITING the ERASE SUSPEND command.

When the ERASE command is WRITTEN during a SECTOR ERASE operation, the device requires a maximum of 20us to SUSPEND the ERASE operation. However, when the ERASE SUSPEND command is WRITTEN during the SECTOR ERASE time-out, the device immediately terminates the time-out period and SUSPENDS the ERASE operation.

After the ERASE operation has been SUSPENDED, the system can READ Array data from or PROGRAM data to any sector not selected for ERASURE. Normal READ and WRITE timings and command definitions apply. READING at any Address within ERASE-SUSPENDED sectors produces status data on three DQ pins within each Byte. DQ2, DQ6, and DQ7 of Byte 1; DQ10, DQ14 and DQ15 of Byte 2; DQ18, DQ22 and DQ23 of Byte 3 as well as DQ26, DQ30 and DQ31 of Byte 4 to determine if a sector is actively ERASING or is ERASE-SUSPENDED.

After and ERASE-SUSPENDED program operation is complete, the system can once again READ from or WRITE to within non-suspended sectors. The system can determine the status of the PROGRAM operation using the DQ6, 7 bits of Byte 1; DQ14, 15 of Byte 2; DQ22, 23 of Byte 3 and DQ30, 31 of Byte 4; just as in the standard PROGRAM operation.

The system may also write the auto select command sequence when the device is in the ERASE SUSPEND mode. The device allows READING autoselect codes even at addresses within

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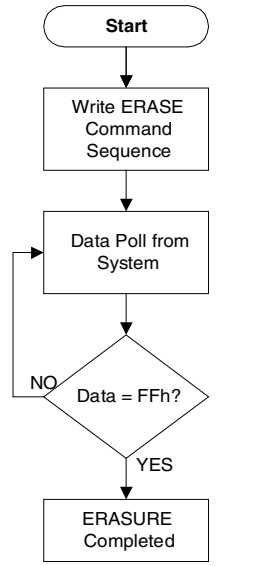
ERASING sectors, since the codes are not stored in the memory Array. When the device exits the Autoselect mode, the device reverts to the ERASE SUSPEND mode, and is ready for another valid operation.

The system must WRITE the ERASE RESUME command to exit the ERASE SUSPEND mode and continue the SECTOR ERASE operation. Further WRITES of the RESUME command are ignored. Another ERASE SUSPEND command can be WRITTEN after the device has resumed ERASING.

Erase Operation Diagram



Write Operation Status

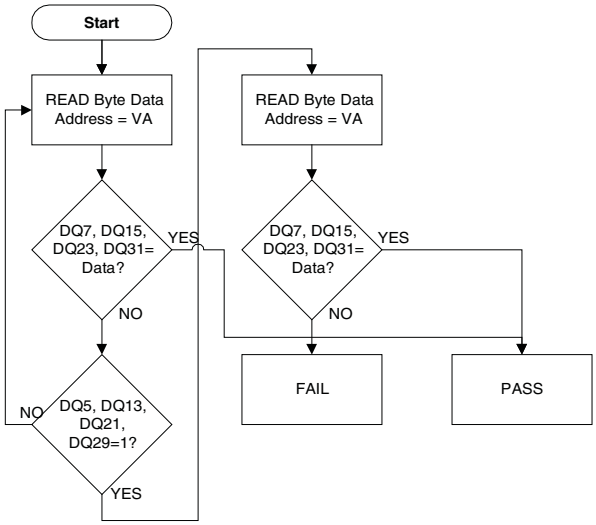
The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6 and DQ7 of Byte 1; DQ10, DQ11, DQ13, DQ14 and DQ15 of Byte 2; DQ18, DQ19, DQ21, DQ22 and DQ23 of Byte 3; as well as, DQ26, DQ27, DQ29, DQ30 and DQ31 of Byte 4.

DQ7, DQ15, DQ23 and DQ31: Data\ Polling

The Data\ Polling bit per byte, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in ERASE SUSPEND. Data\ Polling is valid after the rising edge of the final WEx\ pulse in the PROGRAM or ERASE command sequence.

During the Embedded Program Algorithm, the device outputs on DQ7 for Byte 1, DQ15 for Byte 2, DQ23 for Byte 3, and DQ31
for Byte 4, the complement of the datum programmed to each of these bits. This status also applies to the PROGRAMMING during ERASE SUSPEND. When the Embedded Program

Data\ Polling Algorithm Diagram



Algorithm is complete, the device outputs the datum PROGRAMMED into each of these status bits. The system must provide the PROGRAM address to READ valid status information. If a PROGRAM address fails within a protected sector, Data\ Polling is active for approximately 1uS, then the device returns to reading array data.

During the Embedded Erase Algorithm, Data\ Polling produces a “0” on the Data\ Polling Status bits. When the Embedded ERASE Algorithm is complete, or if the device enters the ERASE SUSPEND mode, Data\ Polling produces a “1” on each of the Data\ Polling status bits. This is analogous to the complement/true data output described for the Embedded Program Algorithm: the ERASE function changes all the bits in a sector to “1”; prior to this, the device outputs the “compliment”, or “0”. The system must provide an address within any of the sectors selected for ERASURE to READ valid status information.

After an ERASE Command sequence is WRITTEN, if all s4ctors selected for erasing are protected, Data\ Polling is active for approximately 100uS, then the device returns to READING array data. If not all selected sectors are protected, the Embedded ERASE Algorithm ERASES the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects a Data\ Polling status bit has changed from the complement to true data, it can READ valid data at each of the Bytes on the following READ cycles. This is because

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Command Definition Table

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2-4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
READ (Note 5)		1	RA	RD										
RESET (Note 6)		1	XXX	F0										
Auto-Select (Note 7)	**Manufacturer ID**	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID, Btm. Boot	4	AAA	AA	555	55	AAA	90	X02	5B				
	Sector Protect Verify (Note 8)	4	AAA	AA	555	55	AAA	90	(SA)	00				
									X04	01				
PROGRAM		4	AAA	AA	555	55	AAA	A0	PA	PD				
UNLOCK BYPASS		3	AAA	AA	555	55	AAA	20						
UNLOCK B (Note 9)		2	XXX	A0	PA	PD								
UNLOCK B (Note 10)		2	XXX	90	PA	00								
CHIP ERASE		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
SECTOR ERASE		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
ERASE SUSPEND (Note 11)		1	XXX	B0										
ERASE RESUME (Note 12)		1	XXX	30										

Legend:

X *= Don't Care*
RA *= Address of the memory location to be READ*
RD *= Data READ from location RA during READ Operation*
PA *= Address of the memory location to be programmed. Addresses latched on the falling edge of WEx\ or CSx\ pulse, whichever occurs later*
PD *= Data to be programmed at location PA. Data latches on the rising edge of WEx\ or CSx\ pulses, whichever occurs later*
SA *= Address of the sector to be VERIFIED (in autoselect mode) or ERASED. Address bits A19-A13 uniquely select any sector*

Notes

1. *See Table 1 for Valid Bus Operations*
2. *All values in Hexadecimal*
3. *Except when READING array or autoselect data, all bus cycles are WRITE Operations*
4. *Address bits A19-A12 are don't cares for UNLOCK and Command cycles*
5. *No UNLOCK or Command cycles required when READING array data*
6. *The RESET command is required to return to READING array data when the device is in the AUTOSELECT mode, or if DQ5, DQ13, DQ21, DQ29 goes high (while the device is providing status data)*
7. *The fourth cycle of the AUTOSELECT Command sequence is a READ Cycle.*
8. *The data is 00h for an unprotected sector and 01h for a protected sector.*
9. *The UNLOCK BYPASS Command is required prior to the UNLOCK BYPASS PROGRAM Command.*
10. *The UNLOCK BYPASS RESET Command is required to return to READING array data when the device is in the UNLOCK BYPASS Mode*
11. *The System may READ and PROGRAM in NON-ERASING sectors, or enter the autoselect mode, when int the ERASE SUSPEND Mode. The ERASE SUSPEND Command is valid only during a sector ERASE Operation*
12. *The ERASE RESUME Command is valid only during the ERASE SUSPEND Mode.*

*Data is for single byte.
BYTE 1 = DQ0 - DQ7
BYTE 2 = DQ8 - DQ15
BYTE 3 = DQ16 - DQ23
BYTE 4 = DQ24 - DQ31

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DQ7, DQ15, DQ23 and DQ31 may change asynchronously with the 7 lower order bits within each Byte, while the OEx\ pins are asserted Low.

DQ6, DQ14, DQ22 and DQ30: Toggle Bit 1

Toggle Bit 1 indicates whether an Embedded Program or Erase Algorithm is in progress, complete, or has entered the ERASE SUSPEND mode. Toggle Bit 1 may be read at any address and is valid after the rising edge of the final WEx\ pulse in the command sequence as well as during the sector ERASE time-out.

During an Embedded Program or Erase Algorithm operation, successive READ cycles that access any address will cause this status indicator to toggle. When the operation is complete, the status bit will stop toggling.

After an ERASE command sequence is WRITTEN, if all sectors selected for ERASING are protected, the toggle bit(s) will toggle for approximately 100uS, then will become steady state as the device returns to READING array data. If not all selected sectors are protected, the Embedded Erase Algorithm will cause ERASURE of unprotected sectors, ignoring the selected sectors that are protected.

The System can use DQ2, DQ6 of Byte 1; DQ10, DQ14 of Byte 2; DQ18, DQ22 of Byte 3; DQ26, DQ30 of Byte 4 together to determine whether a sector is actively ERASING or is ERASE SUSPENDED. When the device is actively ERASING the DQ6 of Byte 1; DQ14 of Byte 2; DQ22 of Byte 3 and DQ30 of Byte 4 toggles and when the devices enters ERASE SUSPEND, the status bit returns to a steady state. However, the system must also use DQ2 of Byte 1; DQ10 of Byte 2, DQ18 of Byte 3 and DQ26 of Byte 4 to determine which sectors are ERASING or ERASE SUSPENDED in each of the Bytes contained in the Module. Alternatively DQ7, DQ15, DQ23 and DQ31 can be used (see DQ7, DQ15, DQ23, DQ31 Data\ Polling).

If a program address falls within a protected sector, DQ6, 14, 22, and or DQ30 will toggle for approximately 1us after the PROGRAM command sequence is WRITTEN, then returns to READING Array data.

DQ6, 14, 22, and or DQ30 also toggles during the ERASE SUSPEND program mode, stops toggling once the operation is complete.

DQ2, DQ10, DQ18 and DQ26: Toggle Bit II

The “Toggle Bit II” on each of the Bytes, when used with DQ6, 14, 22, and DQ30 indicates whether a particular sector is actively ERASING or whether that sector is ERASE-SUSPENDED. Toggle Bit II is valid after the rising edge of the final WEx\ pulse in the command sequence.

DQ2, 10, 18 and or DQ26 toggles when the system READS at addresses within those sectors that have been selected for ERASURE, but does not indicate when a sector is being ERASED. DQ6, 14, 22 and DQ30 by comparison indicates that a device is actively ERASING or in ERASE SUSPEND, but cannot distinguish which sectors are selected for the operation, therefore both status bits are required for sector and mode information.

Reading Toggle Bits I/II

Whenever the system initially begins READING toggle bit statuses, it must READ Byte data (ie…DQ0-7, DQ8-15, DQ16-23 and or DQ24-31) at least twice in a row to determine whether a Toggle Bit is toggling. Typically, the system would note and store the value of the toggle bit after the first READ. After the second READ, the system would compare the new value of the Toggle Bit with the first. If the toggle bit is not toggling the device has completed the PROGRAM or ERASE operation. The system can READ array data on each Byte during the next READ cycle.

If after the initial two READ cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5, 13, 21 and or DQ29 is High. If High, the system should then determine again whether the toggle bit(s) are again toggling, since the toggle bit may have indeed stop toggling just as DQ5, 13, 21 and or DQ29 went High. If the toggle bit is no longer toggling, the device has successfully completed the operation. If the toggle bit is still active (toggling), the device has not successfully completed the operation and the system must WRITE the RESET command to return to READING array data.

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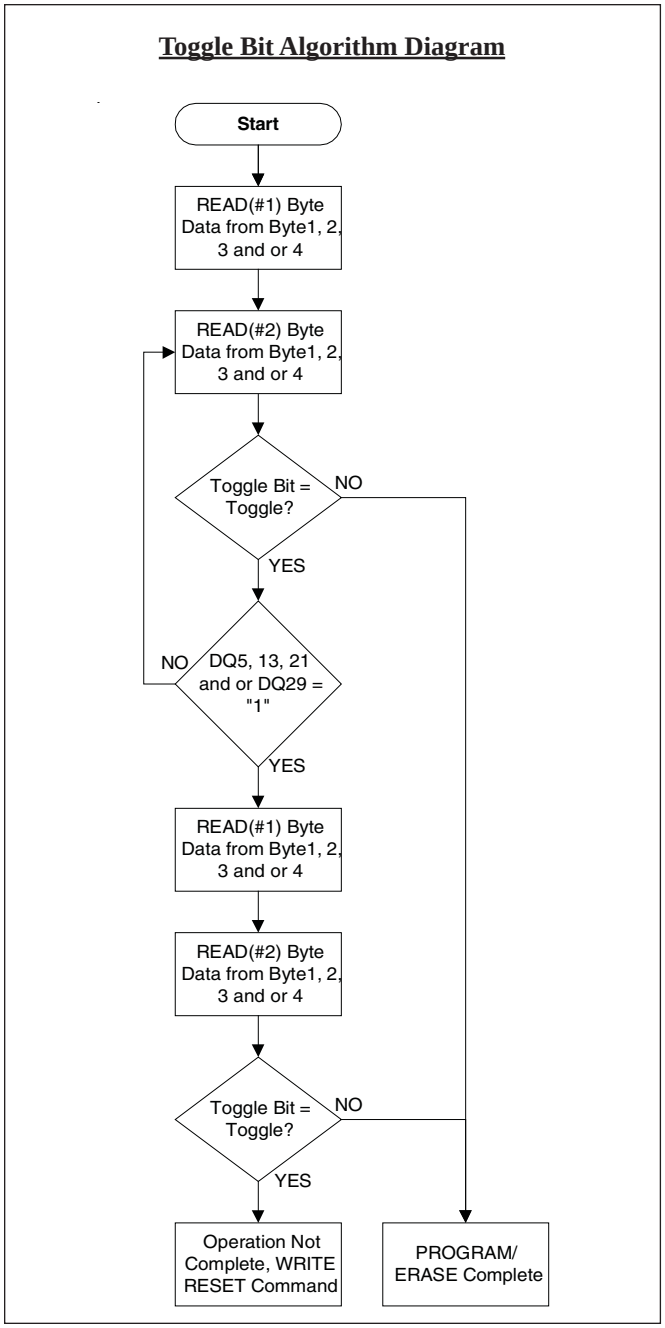
The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5, 13, 21, and or DQ29 has not gone High. The system may continue to monitor the toggle bit and DQ5, 13, 21, and or DQ29 through successive READ cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the Algorithm when it returns to determine the status of the operation.

Toggle Bit Algorithm Diagram



DQ5,13,21,and or DQ29: Exceeding Timing Limits

DQ5, 13, 21, and or DQ29 indicates whether the PROGRAM or ERASE time has exceeded a specified internal pulse count limit. Under these conditions this will produce a logic level "1" High. This is a failure condition that indicates the PROGRAM or ERASE cycle was not successfully completed.

The DQ5, 13, 21 and or DQ29 failure condition may appear if the system tries to PROGRAM a "1" to a location that was previously PROGRAMMED to a logic level "0" Low. Only an ERASE operation can change a logic level "0" back to a Logic Level "1". Under this condition, the device halts operation and when the operation has exceeded the timing limits, DQ5, 13, 21, and or DQ29 will produce a logic level "1".

Under both of these conditions, the system must issue the RESET command to return to reading array data.

DQ3, 11, 19, and or DQ27: Sector Erase Timer

After WRITING a Sector Erase command sequence, the system may read this status bit or bits to determine whether or not an ERASE operation has begun. If additional sectors are selected for ERASURE, the entire time-out also applies after each additional Sector Erase command. When the time-out is complete, this status bit or bits changes from a logic level "0" to "1". The system may ignore this status bit if the system can guarantee that the time between additional Sector Erase command will always be less than 50us.

After the Sector Erase command sequence is WRITTEN, the system should read the status on DQ7, 15, 23 and or DQ31 (Data\ Polling) or DQ6, 14, 22, and or DQ30 (Toggle Bit I) to ensure the device has accepted the command sequence. Then READ DQ3, 11, 19 and or DQ27, looking for this bit or bits to be a logic level "1". If this bit is a logic level "1", the internally controlled ERASE cycle has begun; all further commands are ignored until the ERASE operation is complete. If this bit is a logic level "0", the device will accept additional Sector Erase commands. To ensure the command has been accepted, the system software should check the status of DQ3, 11, 19 and or DQ27 prior to and following each subsequent Sector Erase command. If this bit or bits is a logic level "1" on the second status check, the last command might not have been accepted.

Pin Description/Assignment Table

Signal Name	Symbol	Type	Pin DEF/Package=Q	Symbol	Pin DEF/Package=H	Description
Address	A0, A1, A2. A3, A4, A5, A6, A7 A8, A9, A10, A11 A12,A13,A14,A15 A16,A17,A18,A19	Input	8, 7, 6, 5, 4, 3, 66, 65, 64, 63, 62, 28, 29,30,31,32, 33,37,41,42	A0, A1, A2. A3, A4, A5, A6, A7 A8, A9, A10, A11 A12,A13,A14,A15 A16,A17,A18,A19	7, 60, 61, 62, 49, 50, 51, 37, 41, 17, 16, 6, 38, 40, 4, 18, 5, 28, 8, 21	Address Inputs
Chip Selects	CS1\, CS2\ CS3\, CS4\	Input	34, 36, 2, 68	CS1\, CS2\ CS3\, CS4\	20, 13, 53, 46	Active Low True Chip Selects (Enables)
Write Enables	WE1\, WE2\ WE3\, WE4\	Input	67, 38, 39, 40	WE\	29	Active Low True Write Enable(s)
Output Enable	OE\	Input	35	OE\	27	Active Low True Output Enable (x32)
Reset	RESET\	Input	9	RESET\	12	Active Low True Reset
Power Supply	VCC	Input	61,27	VCC	19, 45	Power for Core and I/O
Ground [Core]	VSS	Input	1,52,18	VSS	14, 54	Digital GND
Data Input, Output	I/O0,I/O1,I/O2 I/O3,I/O4,I/O5 I/O6,I/O7,1/O8 I/O9,I/O10,I/O11 I/O12,I/O13,I/O14 I/O15,I/O16,I/O17 I/O18,I/O19,I/O20 I/O21,I/O22,I/O23 I/O24,I/O25,I/O26 I/O27,I/O28,I/O29 I/O30,I/O31	Input/ Output	10,11,12,13,14,15, 16,17,19,20,21,22, 23,24,25,26,60,59, 58,57,56,55,54,53, 51,50,49,48,47,46, 45,44	I/O0,I/O1,I/O2 I/O3,I/O4,I/O5 I/O6,I/O7,1/O8 I/O9,I/O10,I/O11 I/O12,I/O13,I/O14 I/O15,I/O16,I/O17 I/O18,I/O19,I/O20 I/O21,I/O22,I/O23 I/O24,I/O25,I/O26 I/O27,I/O28,I/O29 I/O30,I/O31	9, 10, 11, 22, 33, 32, 31, 30, 1, 2, 3, 15 26, 25, 24, 23, 42, 43 44, 55, 66, 65, 65, 63 34, 35, 36, 42, 43, 44, 55, 66, 65, 64, 63, 34, 35, 48, 59, 58, 57, 56	Data Input, Output
No Connection	NC	OPEN	43	NC	47, 52, 39	No internal connection

Absolute Maximum Ratings*

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**
Voltage on VDD Pin (Note 1)	VCC	-0.5	4	V
Voltage on A9, OE\, and RESET\ (Note 2)	VCNTL	-0.5	12.5	V
Voltage on Input Pins	VIN	-0.5	VCC+0.5	V
Voltage on I/O Pins	VIO	-0.5	VDDQ+0.5	V
Output Short Circuit Current (Note 3)	ISC		200	mA
Storage Temperature	tSTG	-60	150	°C
Operating Temperatures (Screening Levels)	/IT	-45	85	°C
	/XT	-55	125	°C
Endurance - Write / Erase Cycles	1,000,000 Cycles Min.			
Data Retention	20 Years			

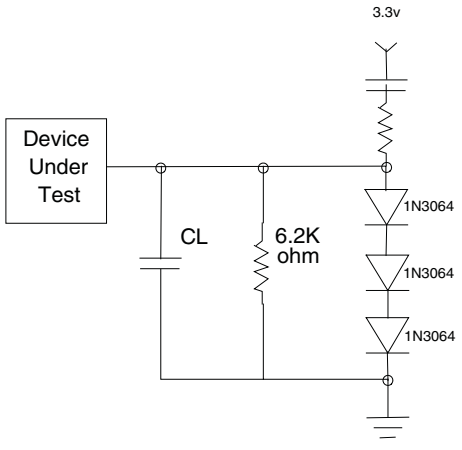
1. *Minimum DC voltage on any Input or Input/Output pin is –0.5v. During voltage transitions, input or input/output pins may undershoot VSS to –2.0v for periods of up to 20ns.*
2. *Minimum DC input/output voltage on pins A9, OE\, and RESET\ is-0.5v. During voltage transitions, A9, OE\, and RESET\ may undershoot VSS to –2.0v for periods of up to 20ns. Maximum DC input voltage on pin A9 is +12.5v which may overshoot to 14.0v for periods up to 20ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one (1) second.*

*Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for any duration or segment of time may affect device reliability.

Test Conditions

Test Specifications				
Parameter		**-70/-90**	**-100/-120**	**Units**
Output Load		1 TTL Gate		
Output Load Capacitance, CL (including Jig)		30	100	pF
Input Rise and Fall Times		5		ns
Input Pulse Levels		0.0-3.0		V
Input timing measurement reference levels		1.5		V
Output timing measurement reference levels		1.5		V

Test Set-Up



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DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units	Notes
ILI	Input Load Current	Vin=Vss to Vcc, Vcc=Vcc MAX			+/- 5.0	uA	
ILIT	A9 Input Load Current	Vcc=Vcc Ma,; A9=12.5v			160.0	uA	
ILO	Output Leakage Current	VOUT=VSS to VCC, VCC=VCC MAX			+/-5.0	uA	
ICC1	Vcc Active Read Current	CE\=VIL, OE\=VIH	14Mhz		120	mA	1,2
			8Mhz		70	mA	1,2
ICC2	VCC Active Write Current	CE\=VIL, OE\=VIH			140	mA	2,3,5
ICC3	VCC Standby Current	CE\, RESET\=VCC +/- 0.3V			150	uA	2
ICC4	VCC Standby Current During Reset	RESET\=VCC +/- 0.3v			150	uA	2
ICC5	Automatic Sleep Mode	VIH=VCC +/- 0.3v, VIL=VSS +/- 0.3v			150	uA	2,4
VIL	Input Low Voltage			-0.5	0.8	V	
VIH	Input High Voltage			0.7xVCC	VCC+0.3	V	
VID	Voltage for Autoselect and Temporary Sector Unprotect	VCC=3.3v		11.5	12.5	V	
VOL	Output Low Voltage	IOL=4.0mA, VCC=VCC MIN			0.45	V	
VOH1	Ouput High Voltage	IOH=-2.0mA, VCC=VCC MIN		2.4		V	
VOH2		IOH=-100uA, VCC=VCC MIN		VCC-0.4			
VLKO	Low VCC Lock-Out Voltage			2.3	2.5	V	4

Notes:

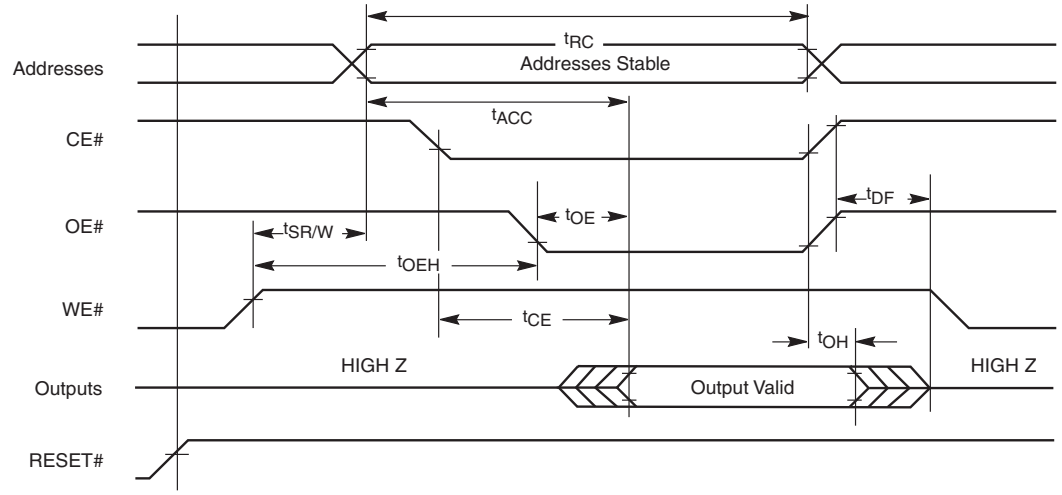
[1] The ICC current listed is typically less than 8mA/Mhz, with OE\ at VIH
[2] Maximum ICC specifications are tested with VCC=VCC MAX
[3] ICC active while Embedded Program or Embedded Erase Algorithm is in progress
[4] Automatic sleep mode enables the low power mode when addresses remain stable for tACC + 30ns
[5] Not 100% Tested

READ Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std					70	90	100	120	
t_{AVAV}	t_{RC}	Read Cycle Time[1]			Min	70	90	100	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	100	120	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = VIL	Max	70	90	100	120	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	35	40	
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z[1]			Max	16				
t_{GHQZ}	t_{DF}	Output Enable to Output High Z[1]			Max	16				
	$t_{SR/W}$	Latency Between Read and Write Operations			Min	20				
	t_{OEH}	Output Enable Hold Time[1]	Read		Min	0				
			Toggle and Data# Polling		Min	10				
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First[1]			Min	0				

Notes:
1. Not 100% Tested

READ Operations Timing



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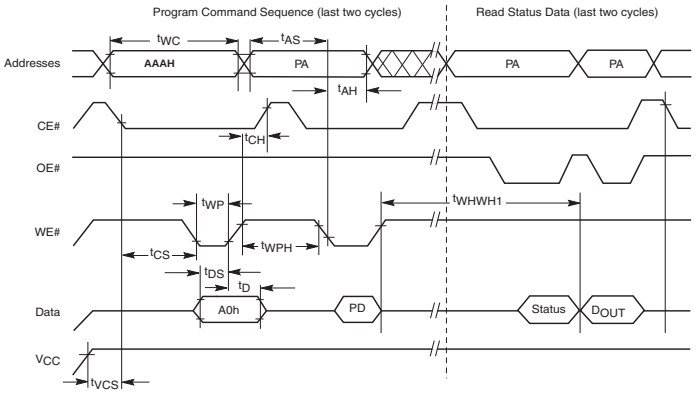
Erase / Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			70	90	100	120	
t_{AVAV}	t_{WC}	Write Cycle Time[1]	Min	70	90	100	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		0				
t_{WLAX}	t_{AH}	Address Hold Time		45				
t_{DVWH}	t_{DS}	Data Setup Time		35	40	45	45	
t_{WHDX}	t_{DH}	Data Hold Time		0				
	t_{OES}	Output Enable Setup Time		0				
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		0				
t_{ELWL}	t_{CS}	CE# Setup Time		0				
t_{WHEH}	t_{CH}	CE# Hold Time		0				
t_{WLWH}	t_{WP}	Write Pulse Width		35				
t_{WHWL}	t_{WPH}	Write Pulse Width High		30				
	$t_{SR/W}$	Latency Between Read and Write Operations		20				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation[2] Byte	Typ	5				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[2]		0.7				sec
	t_{VCS}	Vcc Setup Time[1]	Min	50				µs

Notes:
1. Not 100% Tested
2. See Erase and Programming Performance for more information

Program Operation Timings



Notes
1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.

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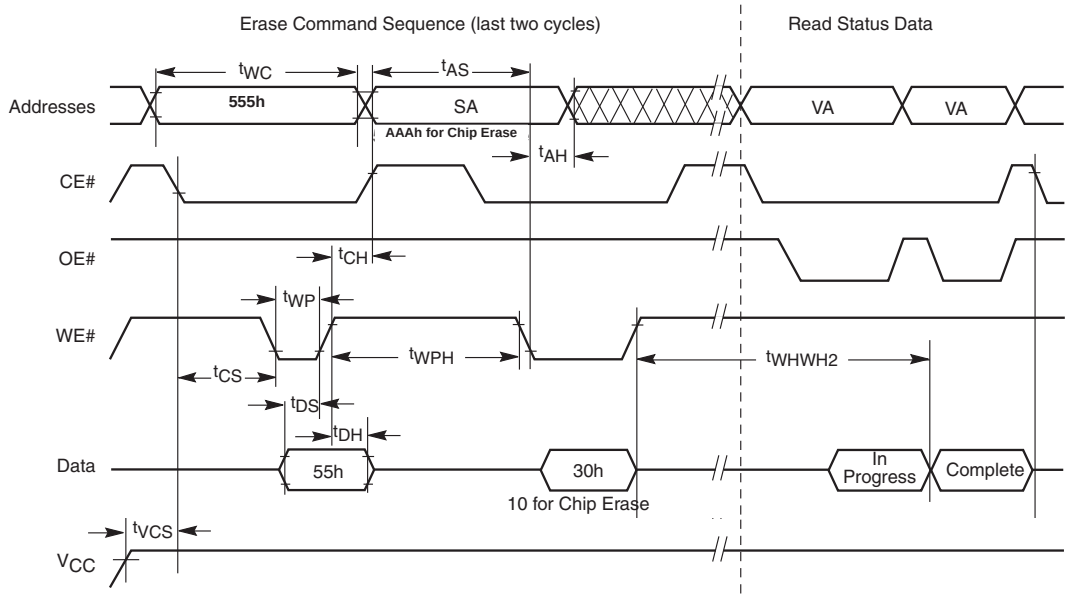
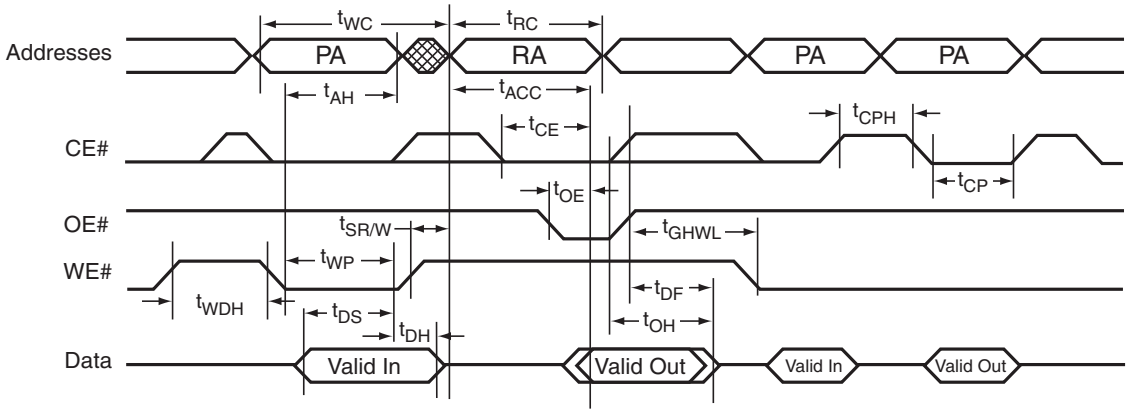
Chip / Sector Erase Operation Timings



Notes:
1. SA=Sector Address (for Sector Erase), VA= Valid Address for reading status data.

Back to Back Read / Write Cycle Timing



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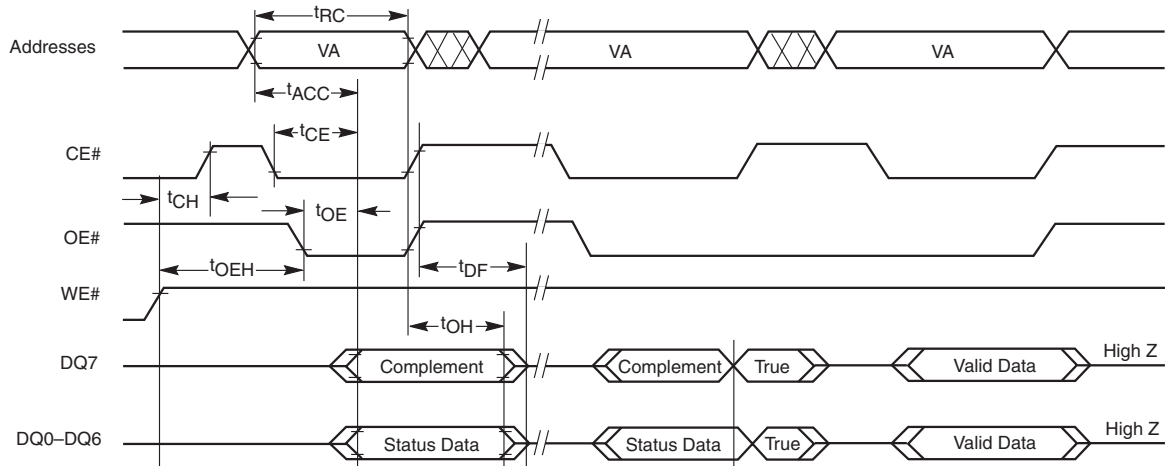
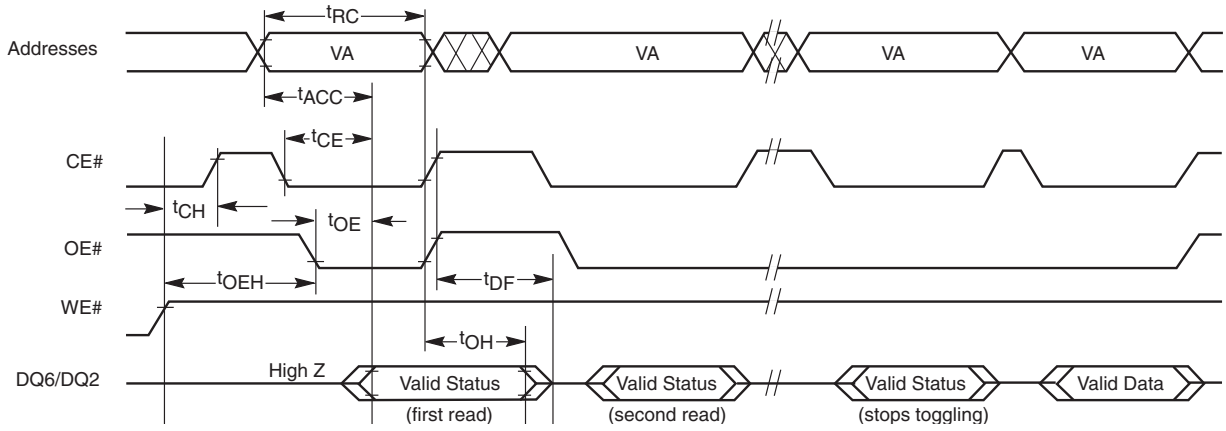
Data# Polling TImings (During Embedded Algorithms)



Note
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

Toggle Bit Timings (During Embedded Algorithms)



Note
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

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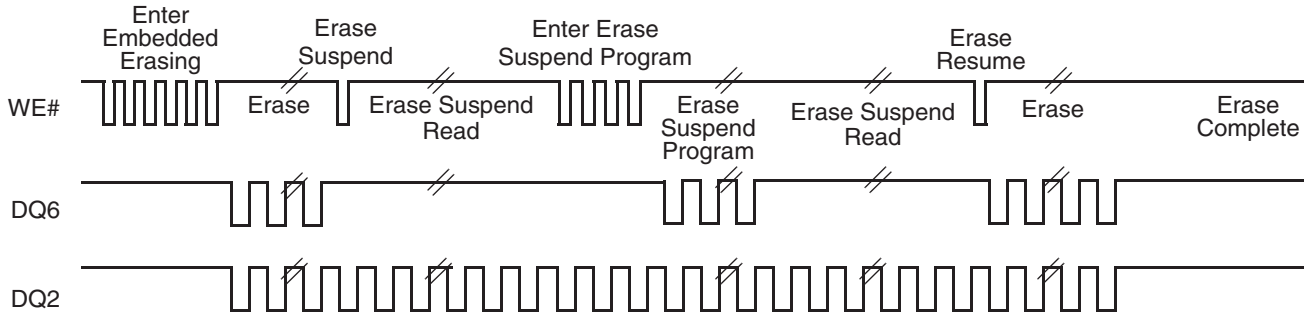
DQ2 vs. DQ6

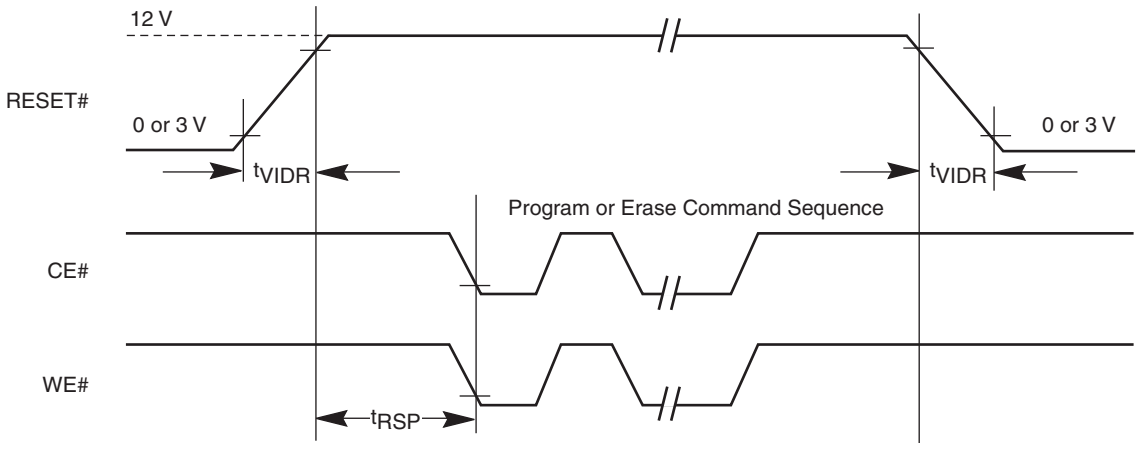


Note
The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time [1]	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Temporary Sector Unprotect Timing Diagram



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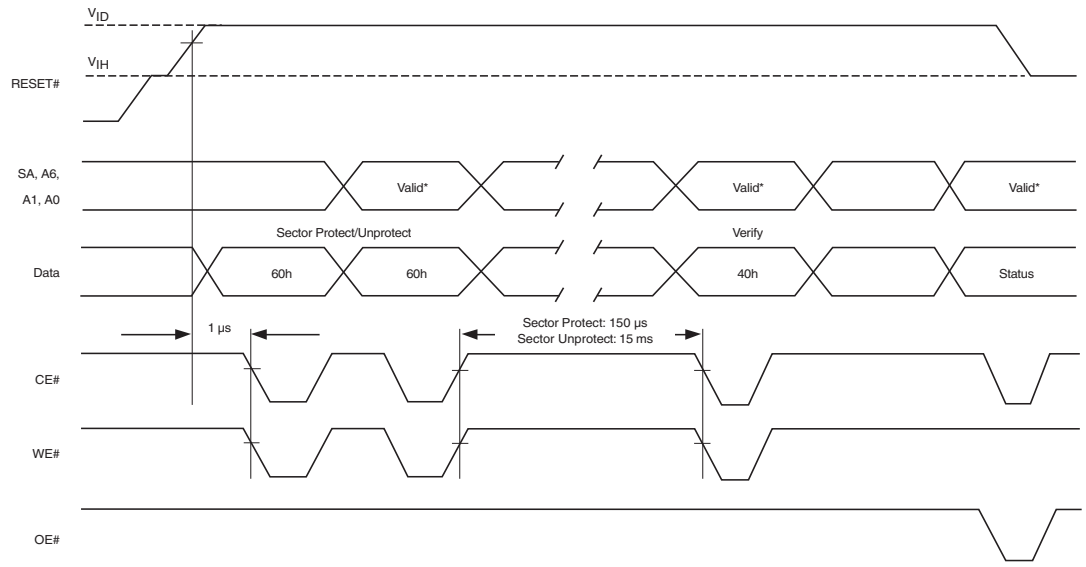
Sector Protect / Unprotect Timing Diagram



Note
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			70	90	100	120	
t_{AVAV}	t_{WC}	Write Cycle Time[1]	Min	70	90	100	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		0				ns
t_{ELAX}	t_{AH}	Address Hold Time		45				ns
t_{DVEH}	t_{DS}	Data Setup Time		35	40	45	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		0				ns
	t_{OES}	Output Enable Setup Time		0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		35				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		30				ns
	$t_{SR/W}$	Latency Between Read and Write Operations		20				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation[2] Byte	Typ	5				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation[2]		0.7				sec

Notes:

1. Not 100% Tested
2. See Erase and Programming Performance

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Hardware Reset (RESET\)

Parameter		Description	Test Setup	All Speed Options	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)	max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		500	ns
	t_{RP}	RESET# Pulse Width	min	500	
	t_{RH}	RESET# High Time Before Read (See Note)		50	
	t_{RPD}	RESET# Low to Standby Mode		20	µs

Note:

Not 100% Tested

Erase and Programming Performance

Parameter		Typ[1]	Max[2]	Unit	Comments
Sector Erase Time		0.7	10	s	Excludes 00h programming prior to erasure
Chip Erase Time		14		s	
Byte Programming Time		7	210	µs	Excludes system level overhead[5]
Chip Programming Time[3]	Byte Mode	8.4	25	s	

NOTES

1. Typical program and erase times assume the following conditions: 25°C, 3.0 V VCC, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.
2. Under worst case conditions of 90°C, VCC = 2.7 V, 1,000,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h be fore erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the pro gram command.
6. The device has a guaranteed minimum erase and program cycle endurance of 1,000,000 cycles.

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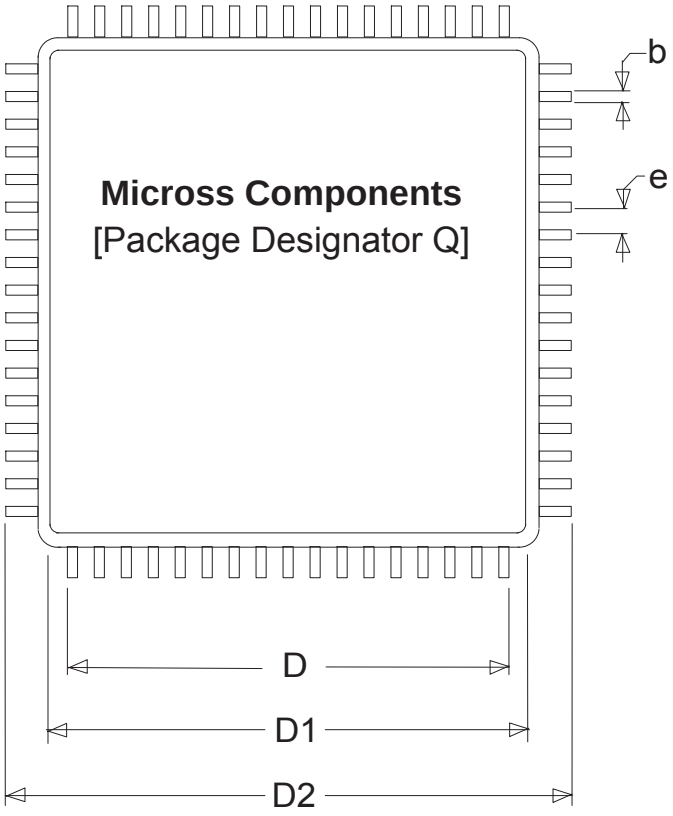
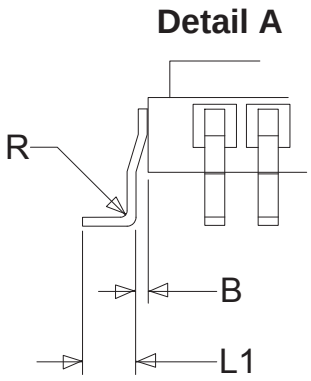
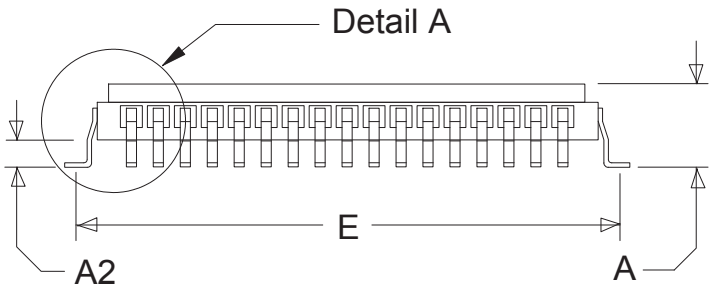
Mechanical Drawings







Package Specifications		
Symbol	Min	Max
A	0.120	0.140
A2	0.005	0.015
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.010 TYP	
L1	0.035	0.045
Dimensions in Inches		

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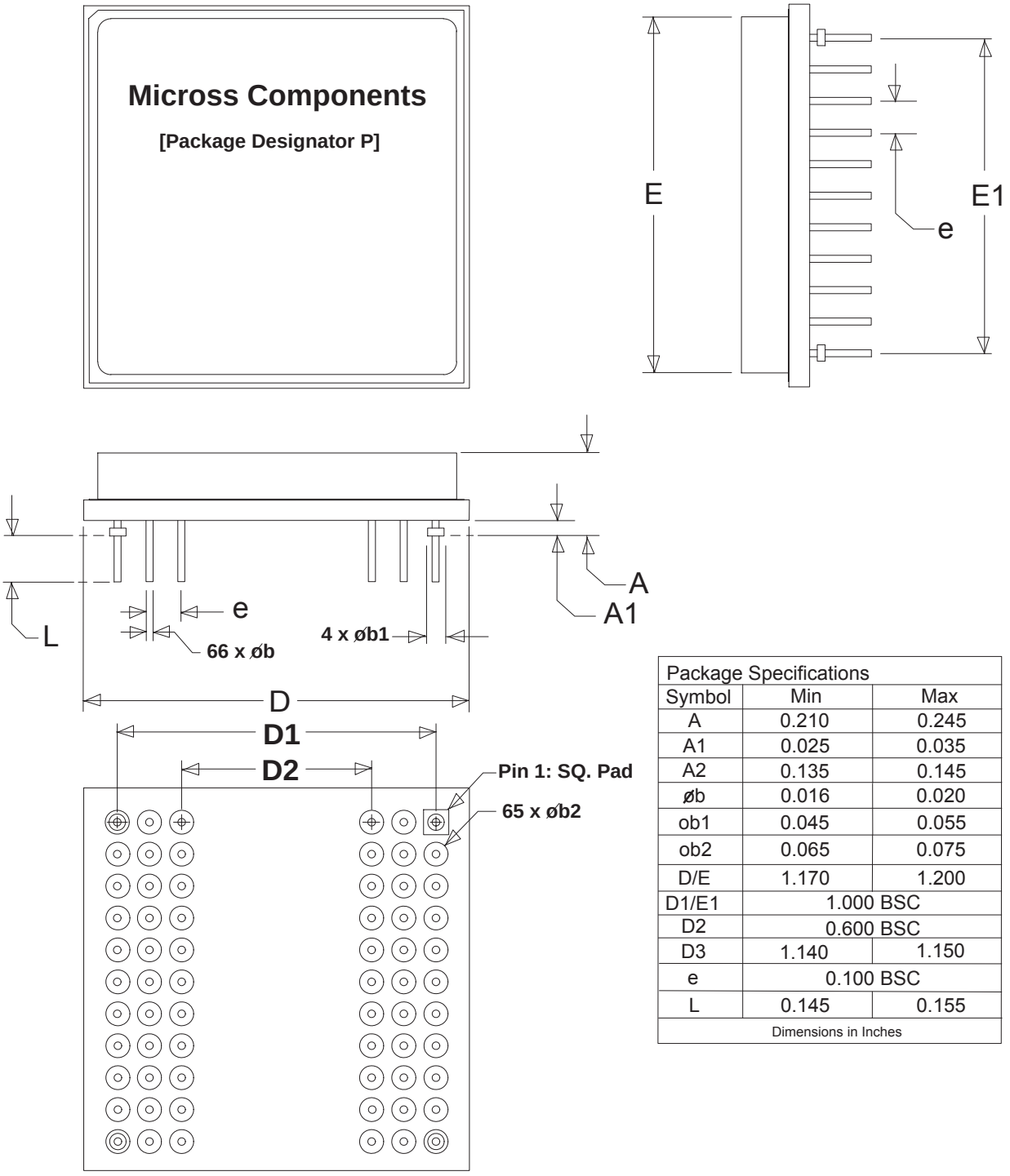
Mechanical Drawings



Package Specifications		
Symbol	Min	Max
A	0.210	0.245
A1	0.025	0.035
A2	0.135	0.145
øb	0.016	0.020
ob1	0.045	0.055
ob2	0.065	0.075
D/E	1.170	1.200
D1/E1	1.000 BSC	
D2	0.600 BSC	
D3	1.140	1.150
e	0.100 BSC	
L	0.145	0.155
Dimensions in Inches		

Ordering Information

Ceramic Quad Flat Pack Micross Part Number	Configuration	Speed (ns)	Pkg.
Industrial Operating Range (-40^{0}C to +85^{0}C)			
AS8FLC1M32BQ-70/IT*	1Mx32, 3.3v,Flash Bottom Boot Block	70	CQFP-68
AS8FLC1M32BQ-90/IT	1Mx32, 3.3v,Flash Bottom Boot Block	90	CQFP-68
AS8FLC1M32BQ-100/IT	1Mx32, 3.3v,Flash Bottom Boot Block	100	CQFP-68
AS8FLC1M32BQ-120/IT	1Mx32, 3.3v,Flash Bottom Boot Block	120	CQFP-68
Extended Operating Range (-55^{0}C to +125^{0}C)			
AS8FLC1M32BQ-70/XT*	1Mx32, 3.3v,Flash Bottom Boot Block	70	CQFP-68
AS8FLC1M32BQ-90/XT	1Mx32, 3.3v,Flash Bottom Boot Block	90	CQFP-68
AS8FLC1M32BQ-100/XT	1Mx32, 3.3v,Flash Bottom Boot Block	100	CQFP-68
AS8FLC1M32BQ-120/XT	1Mx32, 3.3v,Flash Bottom Boot Block	120	CQFP-68
MIL-PRF-38534, CLASS H			
AS8FLC1M32BQ-70/Q*	1Mx32, 3.3v,Flash Bottom Boot Block	70	CQFP-68
AS8FLC1M32BQ-90/Q	1Mx32, 3.3v,Flash Bottom Boot Block	90	CQFP-68
AS8FLC1M32BQ-100/Q	1Mx32, 3.3v,Flash Bottom Boot Block	100	CQFP-68
AS8FLC1M32BQ-120/Q	1Mx32, 3.3v,Flash Bottom Boot Block	120	CQFP-68

Hex Inline Package Micross Part Number	Configuration	Speed (ns)	Pkg.
Industrial Operating Range (-40^{0}C to +85^{0}C)			
AS8FLC1M32BP-70/IT*	1Mx32, 3.3v,Flash Bottom Boot Block	70	HIP-66
AS8FLC1M32BP-90/IT	1Mx32, 3.3v,Flash Bottom Boot Block	90	HIP-66
AS8FLC1M32BP-100/IT	1Mx32, 3.3v,Flash Bottom Boot Block	100	HIP-66
AS8FLC1M32BP-120/IT	1Mx32, 3.3v,Flash Bottom Boot Block	120	HIP-66
Extended Operating Range (-55^{0}C to +125^{0}C)			
AS8FLC1M32BP-70/XT*	1Mx32, 3.3v,Flash Bottom Boot Block	70	HIP-66
AS8FLC1M32BP-90/XT	1Mx32, 3.3v,Flash Bottom Boot Block	90	HIP-66
AS8FLC1M32BP-100/XT	1Mx32, 3.3v,Flash Bottom Boot Block	100	HIP-66
AS8FLC1M32BP-120/XT	1Mx32, 3.3v,Flash Bottom Boot Block	120	HIP-66
MIL-PRF-38534, CLASS H			
AS8FLC1M32BP-70/Q*	1Mx32, 3.3v,Flash Bottom Boot Block	70	HIP-66
AS8FLC1M32BP-90/Q	1Mx32, 3.3v,Flash Bottom Boot Block	90	HIP-66
AS8FLC1M32BP-100/Q	1Mx32, 3.3v,Flash Bottom Boot Block	100	HIP-66
AS8FLC1M32BP-120/Q	1Mx32, 3.3v,Flash Bottom Boot Block	120	HIP-66

*** Contact Factory**

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MICROSS TO DSCC PART NUMBER CROSS REFERENCE FOR 5962-09205*

Micross Package Designator Q		Micross Package Designator P	
Micross Part Number	**SMD Part Number**	**Micross Part Number**	**SMD Part Number**
AS8FLC1M32BQ-70/Q	5962-0920504HXA	AS8FLC1M32BP-70/Q	5962-0920504HYA
AS8FLC1M32BQ-70/Q	5962-0920504HXC	AS8FLC1M32BP-70/Q	5962-0920504HYC
AS8FLC1M32BQ-90/Q	5962-0920503HXA	AS8FLC1M32BP-90/Q	5962-0920503HYA
AS8FLC1M32BQ-90/Q	5962-0920503HXC	AS8FLC1M32BP-90/Q	5962-0920503HYC
AS8FLC1M32BQ-100/Q	5962-0920502HXA	AS8FLC1M32BP-100/Q	5962-0920502HYA
AS8FLC1M32BQ-100/Q	5962-0920502HXC	AS8FLC1M32BP-100/Q	5962-0920502HYC
AS8FLC1M32BQ-120/Q	5962-0920501HXA	AS8FLC1M32BP-120/Q	5962-0920501HYA
AS8FLC1M32BQ-120/Q	5962-0920501HXC	AS8FLC1M32BP-120/Q	5962-0920501HYC

* Micross part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.

DOCUMENT TITLE
32Mb, 1M x 32, 3.3Volt Boot Block FLASH Array

REVISION HISTORY

Rev #	History	Release Date	Status
3.3	Updated Package Information	May 2008	Release
3.4	Changed Package from QT to Q	November 2009	Release
3.5	Changed Package Designator from H to P	November 2009	Release
3.6	Updated Micross Information	January 2010	Release
3.7	Removed all "word" references Added DSCC SMD number for cross reference	February 2010	Release
3.8	Added "Contact Factory" note for -70	February 2010	Release
3.9	Change volt from 3.0 to 3.3	March 2010	Release
4.0	Added data retention data to pg 1 & pg 14	August 2010	Release
4.1	Removed "T" from part number on Cross Reference	October 2010	Release