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RoHS Compliant

Compact Flash 4 Series

Datasheet for Industrial CF

November 17, 2009

Version 1.0

Apacer
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Features:

- **CompactFlash Association Specification Revision 4.1 Standard Interface**
  - 512 bytes per sector
  - ATA command set compatible
  - ATA mode support for up to:
    PIO Mode-6
    Multiword DMA Mode-4
    Ultra DMA Mode-6
- **Capacities**
  - 256, 512 MB
    1, 2, 4, 8, 16 GB
- **Sustained read performance**
  - Up to 50 MB/sec
- **Sustained write performance**
  - Up to 21 MB/sec
- **Flash management**
  - Advanced wear-leveling algorithms to substantially increase longevity of flash media
  - Built-in ECC support for correcting up to 8/15 random single-bit errors per 512-byte sector
  - Read Recovery Technology
  - Power Failure Recovery
  - S.M.A.R.T. Technology
- **NAND Flash Type: SLC**
- **Temperature ranges**
  - Operation: 0°C to 70°C (Standard)
    -40°C to 85°C(ET*)
  - Storage: -40°C to 100°C
- **Support for voltage read and write operations**
  - 3.3 V or 5 V
- **Low power consumption (typical)**
  - Active mode: 95 mA/ 90 mA (3.3 V/ 5 V)
  - Sleep mode: 0.2 mA/ 0.2 mA (3.3 V/ 5 V)
- **Connector Type**
  - 50 pins female
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm
- **RoHS compliant**

*Extended Temperature

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1. General Description

Apacer's Compact Flash 4 offers the most reliable and high performance storage which is compatible with CF Type I and Type II devise. Unlike the others, Apacer Compact Flash 4 provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's Compact Flash 4 complies with the interfaces, such as the commands, timings, and protocols based on the Compact Flash Specification (CFA standard), and operates as the PC Card ATA interface providing complete PCMCIA - ATA functionality and compatibility. Apacer 's Compact Flash 4 is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

1.1 Performance-Optimized Controller

Compact Flash 4 Controller translates standard CF signals into flash media data and control signals.

1.1.1 FIFO Buffer

Compact Flash 4 Controller performs as an FIFO buffer to optimize the host's data transfer to and from the flash media for reliable storage via performing data correction and moving data to another block in case of the correctable error.

1.1.2 Error Correction Code (ECC)

Compact Flash 4 adopts Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to 8/15 random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

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2. Functional Block

Compact Flash 4 Card includes a controller and flash media, as well as the standard Compact Flash interface. Figure 2-1 shows the functional block diagram.

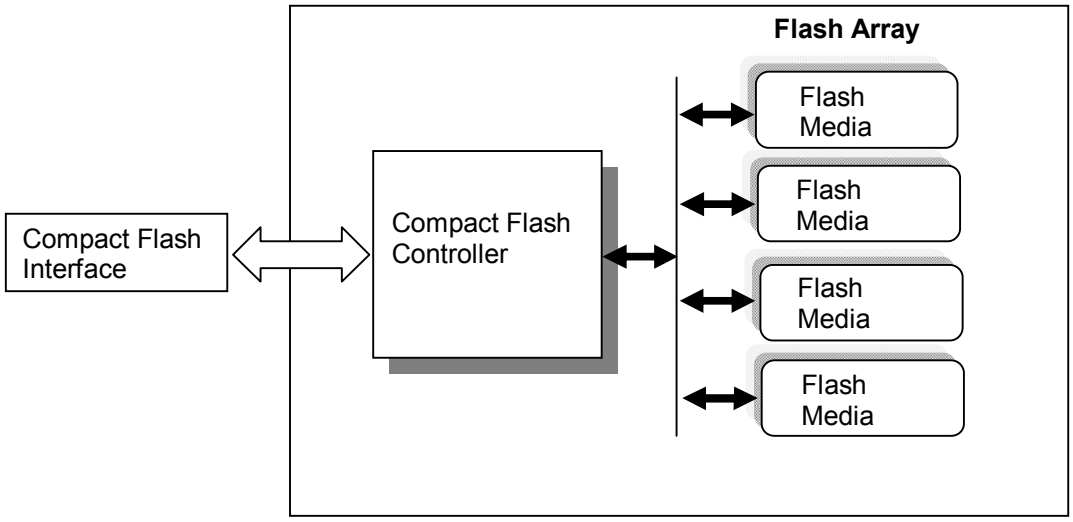

Figure 2-1: Functional block diagram

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3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I

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Table 3-1: Pin assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	#REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	O
46	BVD1	O	#STSCHG	O	#PDIAG	O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

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4. Capacity Specification

Capacity specification of Compact Flash 4 series is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes[1,2]	Cylinders	Heads	Sectors	Max LBA
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1GB	1,024,966,656	1,986	16	63	2,001,888
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,110,188,544	7,964	16	63	8,027,712
8GB	8,195,604,480	15,880	16	63	16,007,040
16GB	16,391,208,960	16,383[3]	16	63	32,014,080

1. Total bytes includes reserved block.
2. Display of total bytes varies from operating systems.
3. Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

4.1 Performance Specification

Performances of Compact Flash 4 are listed below.

Table 4-2: Performance specifications

Capacity / Performance	256 MB	512 MB 1 GB/ 2 GB	4 GB/ 8 GB	16 GB
Sustained read (MB/s)	32	43	46	50
Sustained write (MB/s)	10	15~17	17	21

4.2 Environmental Specifications

Environmental specification of Compact Flash 4 series follows the MIL-STD-810F standards as shown in Table 4-3.

Table 4-3: Environmental specifications

Environment		Specification
Temperature	Operation	0°C to 70°C; -40°C to 85°C (Extended Temperature)
	Storage	-40°C to 100°C
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

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5. Flash Management

5.1 Advanced Wear Leveling

The goal of advanced wear leveling algorithms is to evenly spread the program and erase cycles on the area of programmed and erased multiple times and the area of programmed one and read multiple times among the available blocks in the flash array.

5.2 Read Recovery Technology

Read Recovery Technology enables reliable storage. When it is detected correctable error during read command operation, all data of related block is corrected and is moved to other block. Since it continues to read data after recovery operation, read data is the same as no error data for host system. However, since data transfer is stopped temporarily, the output time of BSY signal becomes long. In order to perform Read Command Recovery, it is necessary to set up the threshold for the number of detected error bit. Read Command Recovery is performed by following commands.

- READ DMA
- READ MULTIPLE
- READ SECTOR(S)
- READ VERIFY SECTOR(S)

5.3 Power Failure Recovery

The controller enables to reduce data loss in case of sudden power fail. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

5.4 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology and enables to expect the endurance of flash memory. The S.M.A.R.T. function protects the user from unexpected fault of product. The S.M.A.R.T function enables to predict the occurrence of near-term degradation or fault conditions by monitoring and storing critical parameters of flash memory (ex. Number of bad block, maximum number of erase, etc). The host system is warned of a negative reliability condition which is the impending risk of data loss by the S.M.A.R.T. function. Then the user can take appropriate action to minimize the risk.

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6. Software Interface

6.1 CF-ATA Command Set

Table 6-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: CFC-ATA command set (1/2)

Command	Code	Command Protocol
CFA Erase-Sector(s)	C0H	Non-data
CFA Request Extended Error Code	03H	Non-data
CFA Translate-Sector	87H	PIO data-in
CFA Write-Multiple-Without-Erase	CDH	PIO data-out
CFA Write-Sector(s)-Without-Erase	38H	PIO data-out
Check-Power-Mode	E5H or 98H	Non-data
Download Microcode	92H	PIO data-out
Execute-Drive-Diagnostic	90H	Device Diagnostic
Flush-Cache	E7H	Non-data
Format-Track	50H	PIO data-out
Identify-Drive	ECH	PIO data-in
Idle	E3H or 97H	Non-data
Idle-Immediate	E1H or 95H	Non-data
Initialize-Drive-Parameters	91H	Non-data
NOP	00H	Non-data
Read-Buffer	E4H	PIO data-in
Read DMA	C8H or C9H	DMA
Read Long	22h or 23h	PIO data-in
Read-Multiple	C4H	PIO data-in
Read-Sector(s)	20H or 21H	PIO data-in
Read-Verify-Sector(s)	40H or 41H	Non-data
Recalibrate	1XH	Non-data
Security Disable Password	F6H	PIO data-out
Security Erase Prepare	F3H	Non-data
Security Erase Unit	F4H	PIO data-out
Security Freeze Lock	F5H	Non-data
Security Set Password	F1H	PIO data-out
Security Unlock	F2H	PIO data-out

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Table 6-1: CFC-ATA command set (2/2)

Command	Code	Command Protocol
Seek	7XH	Non-data
Set-Features	EFH	Non-data
Set-Multiple-mode	C6H	Non-data
Sleep	E6H or 99H	Non-data
SMART Disable Operations	B0H	Non-data
SMART Enable/Disable Attribute Autosave	B0H	Non-data
SMART Enable Operations	B0H	Non-data
SMART Read Attribute Thresholds	B0H	PIO data-in
SMART Read Data	B0H	PIO data-in
SMART Read Log	B0H	PIO data-in
SMART Return Status	B0H	Non-data
Standby	E2H or 96H	Non-data
Standby-Immediate	E0H or 94H	Non-data
Write Buffer	E8H	PIO data-out
Write DMA	CAH or CBH	DMA
Write Long	32H or 33H	PIO data-out
Write Multiple	C5H	PIO data-out
Write Sector(s)	30H or 31H	PIO data
Write Verify	3CH	PIO data
Write Level	F5H	Non-data

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6.1.1 CFA Erase-Sectors(s) – C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (4)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The use of this command in not recommended. This command returns an error.

6.1.2 CFA Request Extended Error Cose – 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests extended error information for the previous command. Table 6-1 defines the valid extended error codes for the device. The extended error code is returned to the host in the Error register.

Table 6-1: Extended Error Codes

Extended Error Code	Description
00H	No Error Detected
01H	Self Test OK (No Error)
09H	Miscellaneous Error
20H	Invalid Command
21H	Invalid Address (Requested Head or Sector Invalid)
2FH	Address Overflow (Address Too Large)
35H, 36H	Supply or generated Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error
05H, 30-34H, 37H, 3EH	Self Test or Diagnostic Failed
10H, 14H	ID Not Found
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media f Format
03H	Write / Erase Failed
22H	Power Level 1 Disabled

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6.1.3 CFA Translate-Sector – 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H or 94H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head, and sector, including its logical address, and the Hot Count, if available, for that sector. Table 5-7 represents the information in the buffer. Please note that this command is unique to the device Controller.

Table 6-2: Translates Sector Information

Address	Information
00H-01H	Cylinder MSB (00), Cylinder LSB (01)
02H	Head
03H	Sector
04H-06H	LBA MSB (04) – LSB (06)
07H-12H	Reserved
13H	Erased Flag (FFh) = Erased; 00h = Not Erased
14H-17H	Reserved
18H-1AH	Hot Count MSB (18) – LSB (1A)[1]
1BH-1FFH	Reserved

1. Mode = transfer mode number, all other values are not valid

6.1.4 CFA Write-Multiple-Without-Erase – CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supposed as Write-Multiple command for backward compatibility.

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6.1.5 Write-Sector(s)-Without-Erase – 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supposed as Write-Multiple command for backward compatibility.

6.1.6 Check-Power-Mode – E5H or 98H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E5H or 98H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode. Because the device can recover from sleep in 200 ns, idle mode is never enabled. Device sets BSY, sets the Sector Count register to 00H, clears BSY and generates an interrupt.

6.1.7 Download Microcode – 92H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	92H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	01H							
Sec Cnt (2)	00H							
Feature (1)	07H							

This command is used to download the microcode to the device. Number of sectors to be downloaded depends on the microcode and should be set to sector count register and sector number register. This command operates regardless of Download Microcode command support (Identify Drive parameter bit 0 of Word 83/86)

6.1.8 Execute-Drive-Diagnostic – 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

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This command performs the internal diagnostic tests implemented by the device. If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices, the Diagnostic codes shown in Table 6-3 are returned in the Error register at the end of the command.

Table 6-3: Diagnostic codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

6.1.9 Flush-Cache – E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the device to complete writing data from its cache. The device then clears BSY and generates an interrupt.

6.1.10 Format-Track – 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (4)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The device expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the device does not use the information in the buffer. The use of this command is not recommended.

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6.1.11 Identify-Drive – ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (4)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the device. This command has the same protocol as the Read- Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 6-4. All reserved bits or words are zero. Table 6-4 is the definition for each field in the Identify-Drive Information.

Table 6-4: Identify-Drive information (1 of 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Reserved
5	0200H	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[2]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-19	ddddH[4]	20	Unique serial number in ASCII
20	0002H	2	Buffer type
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[5]	8	Firmware revision in ASCII.
27-46	ccccH[6]	40	Definable Model number/name
47	8001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH[3]	2	Current numbers of cylinders

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Table 6-4: Identify-Drive information (2 of 2)

Word Address	Default Value	Total Bytes	Data Field Type Information
55	nnnnH[3]	2	Current numbers of heads
56	nnnnH[3]	2	Current sectors per track
57-58	nnnnH[3]	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010X	2	Multiple sector setting
60-61	nnnnH[3]	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Reserved
63	0x07H	2	DMA data transfer is supported in the ATA Disk Module.
64	0003H	2	Advanced PIO Transfer Mode supported
65	0078H	2	120 ns cycle time support for Multiword DMA Mode-2
66	0078H	2	120 ns cycle time support for Multiword DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	007EH	2	ATA/ATAPI major version number
81	0019H	2	ATA/ATAPI minor version number
82	706BH	2	Features/command sets supported
83	400CH	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	xx1FH	2	UDMA mode
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91-127	0000H	72	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-162	000H	6	Reserved
163	xx2H	2	Reserved
164-255	0000H	190	Reserved

1. XXXX=This field is subject to change by the host or the device
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. dddd - unique number of each device
5. aaaa - any unique firmware revision
6. cccc - default value is “xxxMB” where xxx is the device capacity.
   The user has an option to change the model number during manufacturing.

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- **Word 0: General Configuration**

  This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MB/sec and is not MFM encoded.

- **Word 1: Default Number of Cylinders**

  This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

- **Word 3: Default Number of Heads**

  This field contains the number of translated heads in the default translation mode.

- **Word 6: Default Number of Sectors per Track**

  This field contains the number of sectors per track in the default translation mode.

- **Word 7-8: Number of Sectors**

  This field contains the number of sectors per device. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

- **Word 10-19: Serial Number**

  Unique serial number ID. The twenty bytes are a user-programmable value with a default value of spaces.

- **Word 20: Buffer Type**

  This field defines the buffer capability:
  0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the Device.

- **Word 23-26: Firmware Revision**

  This field contains the revision of the firmware for this product.

- **Word 27-46: Model Number**

  This field contains the model number for this product.

- **Word 47: Read-/Write-Multiple Sector Count**

  This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

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- **Word 49: Capabilities**

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: PIO Mode-4 is supported.
9	LBA Support 1: LBA mode addressing is supported.
8	DMA Support 1: DMA mode is supported.

- **Word 51: PIO Data Transfer Cycle Timing Mode**

  This field defines the mode for PIO data transfer. The Device module supports up to PIO Mode-

- **Word 53: Translation Parameters Valid**

Bit	Function
0	1: Words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: Words 64-70 are valid to support PIO Mode-3 and 4.
2	1: Word 88 is valid to support Ultra DMA data transfer.

- **Word 54-56: Current Number of Cylinders, Heads, Sectors/Track**

  These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

- **Word 57-58: Current Capacity**

  This field contains the product of the current cylinders times heads times sectors.

- **Word 59: Multiple Sector Setting**

  This field contains a validity flag in the Odd Byte and the current numbers of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

  The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

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- **Word 60-61: Total Sectors Addressable in LBA Mode**

  This field contains the number of sectors addressable for the Device in LBA mode only.

- **Word 63: Multiword DMA Transfer**

  This field identifies the Multiword DMA transfer modes supported by the Device module and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time.

Bit	Function
15-11	Reserved
10	Multiword DMA mode-2 selected 1: Multiword DMA mode-2 is selected and bits 8 and 9 are cleared to 0. 0: Multiword DMA mode-2 is not selected.
9	Multiword DMA mode-1 selected 1: Multiword DMA mode-1 is selected and 8 and 10 shall be cleared to 0. 0: Multiword DMA mode-1 is not selected.
8	Multiword DMA mode-0 selected 1: Multiword DMA mode-0 is selected and bits 9 and 10 are cleared to 0. 0 then Multiword DMA mode-0 is not selected.
7-3	Reserved
2	Multiword DMA mode-2 supported 1: Multiword DMA mode-2 and below are supported and Bits 0 and 1 shall be set to 1.
1	Multiword DMA mode-1 supported 1: Multiword DMA mode-1 and below are supported.
0	Multiword DMA mode-0 supported 1: Multiword DMA mode-0 is supported.

- **Word 64: Advanced PIO Data Transfer Mode**

  Bit (7:0) is defined as the PIO data and register transfer supported field. If this field is supported, Bit 1of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bit (7:2) are Reserved for future PIO modes.

Bit	Function
0	1: PIO Mode-3 is supported.
1	1: PIO Mode-4 is supported.

- **Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word**

  This field defines the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the Device supports when performing Multiword DMA transfers on a per word basis. The Device supports up to Multiword DMA Mode-2, so this field is set to 120ns.

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- **Word 66: Device Recommended Multiword DMA Cycle Time**

  This field defines the Device recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the Device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. The Device supports up to Multiword DMA Mode-2, so this field is set to 120ns.

- **Word 67: Minimum PIO Transfer Cycle Time Without Flow Control**

  This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The Device minimum cycle time is 120 ns. A value of 0078H is reported.

- **Word 68: Minimum PIO Transfer Cycle Time with IORDY**

  This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfer while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The Device minimum cycle time is 120 ns, e.g., PIO mode 4. A value of 0078H is reported.

- **Word 80: Major Version Number**

  If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. The Device supports ATA-1 to ATA-6.

- **Word 81: Minor Version Number**

  If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 shall be 0000H or FFFFH.

  A value of 0019H reported in word 81 indicates ATA/ATAPI-6 T13 1410D revision 3a guided the implementation.

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- **Words 82-84: Features/command sets supported**

  Words 82, 83, and 84 indicate the features and command sets supported.

  Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	0: SMART feature set is not supported

  Word 83

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are not valid
14	1: Provides indications that the features/command sets supported words are valid
13-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is not supported
2	1: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	1: Download Microcode command is not supported

  Word 84

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-0	0: Reserved

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- **Words 85-87: Features/command sets enabled**

  Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

  Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0: Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is not enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

  Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled via the Set Features command 1: Advanced Power Management feature set is enabled via the Set Features command
2	0: CFA feature set is disenabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

  Word 87

  The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-0	0: Reserved

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Word 88

Bit	Function
15-13	Reserved
12	1: Ultra DMA mode-4 is selected 0: Ultra DMA mode-4 is not selected
11	1: Ultra DMA mode-3 is selected 0: Ultra DMA mode-3 is not selected
10	1: Ultra DMA mode-2 is selected 0: Ultra DMA mode-2 is not selected
9	1: Ultra DMA mode-1 is selected 0: Ultra DMA mode-1 is not selected
8	1: Ultra DMA mode-0 is selected 0: Ultra DMA mode-0 is not selected
7-5	Reserved
4	1: Ultra DMA mode-4 and below are supported
3	1: Ultra DMA mode-3 and below are supported
2	1: Ultra DMA mode-2 and below are supported
1	1: Ultra DMA mode-1 and below are supported
0	1: Ultra DMA mode-0 is supported

- **Word 89: Time required for Security erase unit completion**

  Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

- **Word 90: Time required for Enhanced security erase unit completion**

  Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

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- **Word 128: Security Status**

Bit	Function
8	Security Level 1: Security mode is enabled and the security level is the maximum 0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked
1	Enable/Disable 1: Security is enabled 0: Security is disabled
0	Capability 1: supports security mode feature set 0: does not support security mode feature set

6.1.12 Idle – E3H or 97H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3H or 97H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5msec increments)							
Feature (1)	X							

This command causes the Device to set BSY, enter the Idle Mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero and the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5ms. Note that this time base (5msec) is different from the ATA specification.

6.1.13 Idle-Immediate – E1H or 95H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1H or 95H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Device to set BSY, enter the Idle Mode, clear BSY and generate an interrupt.

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6.1.14 Initialize-Drive-Parameters – 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

6.1.15 NOP – 00H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	00H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command always fails with the device returning command aborted.

6.1.16 Read-Buffer – E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Buffer command enables the host to read the current contents of the Device's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.1.17 Read DMA – C8H or C9H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8H or C9H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to the READ SECTOR (S) command except for the following:

- The host initializes the DMA channel prior to issuing the command;
- Data transfers are qualified by DMARQ and are performed by the DMA channel;
- The device issues only one interrupt per command to indicate that data transfer has terminated and

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status is available.

During the DMA transfer phase of a READ DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The flawed data is pending in the sector buffer. Subsequent sectors are transferred only if the error was a correctable data error. All other errors cause Read-DMA to stop after transfer of the sector that contained the error.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

6.1.18 Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22H or 23H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the device does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.1.19 Read-Multiple – C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The Read- Multiple command is similar to the Read- Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set-Multiple command.

Command execution is identical to the Read- Sectors operation except that the numbers of sectors defined by a Set-Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Read- Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer.

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The partial block transfer is for n sectors, where n = remainder (sector count/block count). If the Read-Multiple command is attempted before the Set-Multiple Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read- Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector counts of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

6.1.20 Read Sectors – 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sectors count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Device sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.1.21 Read Verify Sector(s) – 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

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This command is identical to the Read- Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Device sets BSY.

When the requested sectors have been verified, the Device clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

6.1.22 Recalibrate – 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X	LBA	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation command to the device and is provided for compatibility purposes.

6.1.23 Security-Disable-Password – F6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests a transfer of a single sector of data from the host. Table 6-5 defines the content of this sector of information. If the password selected by Word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 6-5: Security password data content

Word	Content
0	Control word: Bit 0: Identifier 0: Compare user password 1: Compare master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-256	Reserved

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6.1.24 Security-Erase-Prepare – F3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is issued immediately before the Security-Erase-Unit command to enable device erasing and unlocking. This command prevents accidental erasure of the data in the flash media.

6.1.25 Security-Erase-Unit – F4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests transfer of a single sector of data from the host. Table 6-5 defines the content of this sector of information. If the password does not match the password previously saved by the device, the device rejects the command with command aborted. The Security-Erase-Prepare command should be completed immediately prior to the Security-Erase-Unit command. If the device receives a Security-Erase-Unit command without an immediately prior Security-Erase-Prepare command, the device aborts the Security- Erase-Unit command.

6.1.26 Security-Freeze-Lock – F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Security-Freeze-Lock command sets the device to Frozen mode. After command completion, any other commands that update the device Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security-Freeze-Lock is issued when the device is in Frozen mode, the command executes and the device remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0. Commands disabled by Security-Freeze-Lock are:

- Security-Set-Password
- Security-Unlock
- Security-Disable-Password
- Security-Erase-Unit

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If security mode feature set is not supported, this command shall be handled as Wear- Level command.

6.1.27 Security-Set-Password – F1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F1H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests a transfer of a single sector of data from the host. Table 6-6 defines the content of the sector of information. The data transferred controls the function of this command.

Table 6-6: Security password data content

Word	Content
0	Control word: Bit 0: Identifier 0: Compare user password 1: Compare master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-256	Reserved

Table6-7: Identifier and security level bit interaction

Identifier	Level	Command Result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock mode shall be enabled from the next power-on reset or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device shall not be used to unlock the device.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

6.1.28 Security-Unlock – F2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F2H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

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This command requests transfer of a single sector of data from the host. Table 6-7 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security-Unlock is issued and the device is locked. Once this counter reaches zero, the Security-Unlock and Security-Erase-Unit commands are command aborted until after a power-on reset or a hardware reset is received. Security-Unlock commands issued when the device is unlocked have no effect on the unlock counter.

6.1.29 Seek – 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a NOP command to the Device although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.1.30 Set-Features – EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 6-8 defines all features that are supported.

Table 6-8: Features supported (1/2)

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 4-9 defines the values.
09H	Enable Extended Power Operations
55H	Disable Read Look Ahead.
66H	Disable Power- on Reset (POR) establishment of defaults at software Reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.

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Table 6-8: Features supported (2/2)

Feature	Operation
82H	Disable Write Cache
89H	Disable Extended Power operations
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
AAH	Enable Read Look Ahead.
CCH	Enable Power- on Reset (POR) establishment of defaults at software Reset.

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the Device that implement write cache. When the subcommand Disable-Write-Cache is issued, the Device should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the ATA Disk Module. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

Table 6-9: Transfer mode values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multiword DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

1. Mode = transfer mode number, all other values are not valid

6.1.31 Set-Multiple-Mode – C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

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This command enables the Device to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the Device sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted command error is posted, and Read- Multiple and Write- Multiple commands are disabled. If the Sector Count registers contains 0 when the command is issued, Read and Write- Multiple commands are disabled. At power-on, or after a hardware or (unless disabled by a Set-Feature command) software reset, the default mode is Read and Write-Multiple disabled.

6.1.32 Sleep – E6H or 99H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6H or 99H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

6.1.33 SMART – B0H

The feature register will indicate the subcommand as listed below.

- **6.1.33.1 SMART Return Status – DAH**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	DAH							

Command Purpose:
This Command is used to communicate the reliability status of the device to the host at the host's request. If the device has not detected a threshold exceeded condition, the device sets the LBA Mid register to 4FH and the LBA High register to C2H. If the device has detected a threshold exceeded condition, the device sets the LBA Mid register to F4H and the LBA High register to 2CH. In the current implementation, the only threshold checked is that a fatal error has occurred.

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- **6.1.33.2 SMART Enable/Disable Attribute Autosave – D2H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	00H or F1H							
Feature (1)	D2H							

Command Purpose:
This Command enables or disables the optional attribute autosave feature of the device. A value of 00H in the Sec Cnt register will disable the autosave feature. A value of F1H in the Sec Cnt register will enable the autosave feature. Currently, no action is generated by this command since there in no online collection of data.

- **6.1.33.3 SMART Enable Operations – D8H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D8H							

Command Purpose:
This Command enables access to all SMART capabilities within the device. Prior to receipt of this command, SMART data is collected but not accessible via SMART. The state of SMART (either enabled or disable) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

- **6.1.33.4 SMART Disable Operations – D9H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D9H							

Command Purpose:
This Command disables access to SMART data via SMART commands. After receipt of this command the device shall disable all SMART operations. However SMART data shall continue to be collected and accessible when SMART is next enabled. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. After receipt of this command by the device, all other SMART commands, including SMART DISABLE OPERATIONS commands, with the exception of SMART ENABLE OPERATIONS, are disabled and invalid, and the commands shall aborted by the device.

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- **6.1.33.5 SMART Execute Offline – D4H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	Subcommand Specific							
Sec Cnt (2)	X							
Feature (1)	D4H							

Command Purpose:
This Command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and the save this data to the device's memory. This data is not retained across resets and a new command must be executed to recollect data. The SMART data collected is determined by the subcommand specified in the Sec Num register. All subcommands other than listed below will be aborted. Valid subcommands will be executed in captive mode and the device will set BSY bit until command is completed. The collected data should be read by a subsequent SMART Read Data (D0H) command.

Table 6-10: SMART EXECUTE OFF-LINE Sector Number register values (sub-command specific)

Subcommand	Collected Data
0-201	Reserved
202 (0xCA)	Bad block count (captive)
203 (0xCB)	Group free block count (captive)
204 (0xCC)	Group average age (captive)
205 (0xCD)	Group maximum age (captive)
206 (0xCE)	Group minimum age (captive)
207 (0xCF)	Group wear swap count (captive)
208 (0xD0)	Group retention swap count (captive)
209 (0xD1)	Group total block erase count (captive)
210-255	Reserved

- **6.1.33.6 SMART Read Data – D0H**

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D0H							

Command Purpose:
This Command returns the device SMART data structure to the host. This command must be preceded by the SMART Execute Offline command with an appropriate subcommand listed above. The returned data will depend on the requested subcommand.

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All returned data comply with the SMART data structure as specified in the ATA spec. Bytes 0 to 361 of the structure returns vendor specific data that depends of the requested subcommand. Bytes 362 to 385 are standard values as defined in the ATA spec. bytes 386 to 510 returns vendor specific data common to all subcommands. Byte 511 is the 2's complement checksum of all bytes in the data structure.

Offline Data Collection Status (byte 362)

The offline data collection status byte indicates whether SMART data collection was successful or not. The host should check this value in the returned data structure before proceeding with interpretation of vendor specific data bytes. The follow are possible status values.

Value	Definition
00H	Offline data collection activity was never started.
02H	Offline data collection activity was completed without error.
04H	Offline data collection activity was suspended host.
05H	Offline data collection activity was aborted by host.
06H	Offline data collection activity was aborted by device.

6.1.34 Standby – E2H or 96H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2H or 96H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

6.1.35 Standby-Immediate – E0H or 94H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H or 94H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the Device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

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6.1.36 Write-Buffer – E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the Device sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 byes.

6.1.37 Write-DMA – CAH or CBH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAH or CBH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to Write-RITE Sector(s) except for the following:

- The host initializes the DMA channel prior to issuing the command

- Data transfers are qualified by DMARQ and are performed by the DMA channel

- The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write-RITE DMA command, the device shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs after the attempted write of a transferred sector, the command is terminated and subsequent blocks are not transferred. The command block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors for successful completion of the command.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

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6.1.38 Long –32H or 33H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32H or 33H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA23-16)							
Cyl Low (4)	Cylinder Low (LBA15-8)							
Sec Num (3)	Sector Number (LBA7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state device, the four bytes of ECC transferred by the host may be used by the device. The device may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

6.1.39 Write-Multiple – C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High (LBA23-16)							
Cyl Low (4)	Cylinder Low (LBA15-8)							
Sec Num (3)	Sector Number (LBA7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the Device can support up to a block count of 1 as indicated in the Identify Drive Command information.

This command is similar to the Write-Sectors command. The Device sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set-Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set-Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where: n = remainder (sector count/block count).

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

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The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

6.1.40 Write-Sector(s) – 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-89)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the Device sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host. For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.1.41 Write-Verify – 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

6.1.42 Wear Level – F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

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For the device that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register shall always be returned with a 00h indicating Wear Level is not needed. If the device supports security mode feature set, this command shall be handled as Security Freeze Lock.

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7. Electrical Specification

7.1 Absolute Maximum Ratings

Caution: **Absolute Maximum Ratings –** Applied conditions greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 7-1: Absolute maximum ratings

(Based on GND [0V])

Item	Symbol	Rated Value	Unit	Condition
Power supply voltage	VDDIO	-0.5~+4.6	V	
Input voltage	V_{IN}(Standard)	-0.5~+4.6	V	V_{IN} < VDDIO+0.5V
	V_{IN}(5V-Tolerant)	-0.5~+6.6 (The power is supplied)	V	V_{IN} < VDDIO+3V
Output current	I_{OUT}	±11	mA	3mA buffer
		±21	mA	6mA buffer
		±29	mA	9mA buffer
		±45	mA	12mA buffer
Storage temperature	T_{STG}	-40~+100	℃	

7.2 Recommended Operating Conditions

Table 7-2: Recommended Operating Conditions

Item	Symbol	Rated Value	Unit	Condition
Input voltage	V_{IN}(Standard)	2.7~3.6	V	
	V_{IN}(5V-Tolerant)	4.5~5.5	V	
Operating ambient temperature	T_A	-40~+85	℃	

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7.3 DC Characteristics

Table 7-3: DC Characteristics (@ VDDIO=3.3V)

Item	Symbol	Standard Value			Unit	Measurement Condition
		Min	Typ	Max		
Input voltage (TTL level)	VIH	2.0	—	VDDIO	V	
	VIL	0	—	0.7	V	VDDIO=2.7V
Schmidt trigger input (TTL level)	V+	1.2	—	2.4	V	
	V-	0.6	—	1.8	V	
	Vh	0.3	—	1.5	V	
Output voltage	VOH	VDDIO-0.1	—	—	V	IOH=0mA
	VOL	—	—	0.1	V	IOL=0mA
Input leak current	IIH	-10	—	+10	uA	VIN=VDDIO
	IIL	-10	—	+10	uA	VIN=VSS
Output leak current	IOZ	-10	—	+10	uA	Hi-Z state
Pull-up resistance	RPU	14.2	31.9	80.7	kΩ	VIN=VSS
Pull-down resistance	RPD	20.6	44.9	116.4	kΩ	VIN=VDDIO
Current consumption (VDDIO)	ICC33udma6	—	40	—	mA	UDMA mode 6 (when 2ch interleave)
	ICC33pio6	—	20	—	mA	PIO mode 6 (when 2ch interleave)
	ICC33idl	—	2	—	mA	IDLE
	ICC33slp	—	0.1	—	mA	SLEEP

7.4 Capacitance

Table 7-4: Capacitance

Item	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance (5V-Tolerant)	Ci (5V-Tolerant)	7	—	11	pF
I/O Pin Capacitance (5V-Tolerant)	Cio (5V-Tolerant)	7	—	11	pF

7.5 Integrated Series Termination Resistor

Table 7-5: Integrated Series Termination Resistor

Item	Symbol	Min	Typ	Max	Unit
Terminator Resistance	Rterm	27	33	39	Ω

INTRQ, #INPACK, IORDY, DMACK, #CS0, #CS1, #IORD, #IOWR, A[2:0] and D[15:0] (IDE mode) signals that have integrated series termination resistors.

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7.6 Power Supply Sequence

The controller is an IC that functions at 3.3V for the I/O power supply. There power supplies will deliver power to the chip externally, but a through current may occur inside the chip depending on the power-on and power-off sequence. For this reason, the power supply should be turned on and off simultaneously for reliability. Refer to figure 7-1.

- Turn on condition
  Time difference of VDDIO*0 to both VDDIO*0.9 is less than 100[ms].
- Turn off condition
  Time difference of VDDIO*0.9 to both VDDIO*0.1 is less than 100[ms].
- 5V tolerant buffer
  Before/after power supply is turned on/off, it must not apply 5V voltage.

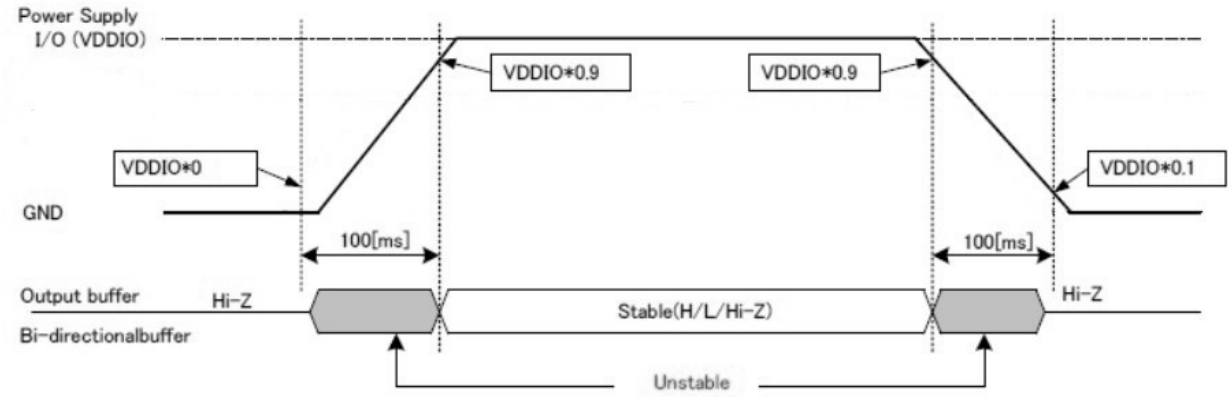

Figure 7-1 Power ON/OFF Sequence

7.7 Setup Time

Hardware reset time (reset release to a ready state) is less than about 100 [ms] in PC Card/HOST Memory Bus mode. For IDE mode, it is less than about 450 [ms] when master connection, and is less than about 250 [ms] when slave connection. Setup time does not depend on the total capacity of connected flash memory.

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8. Physical Characteristics

8.1 Dimension

TABLE 8-1: Type I CFC physical specification

Length:	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
Width:	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
Thickness (Including Label Area):	3.3mm+/-0.10mm (0.130+/-0.04in.)

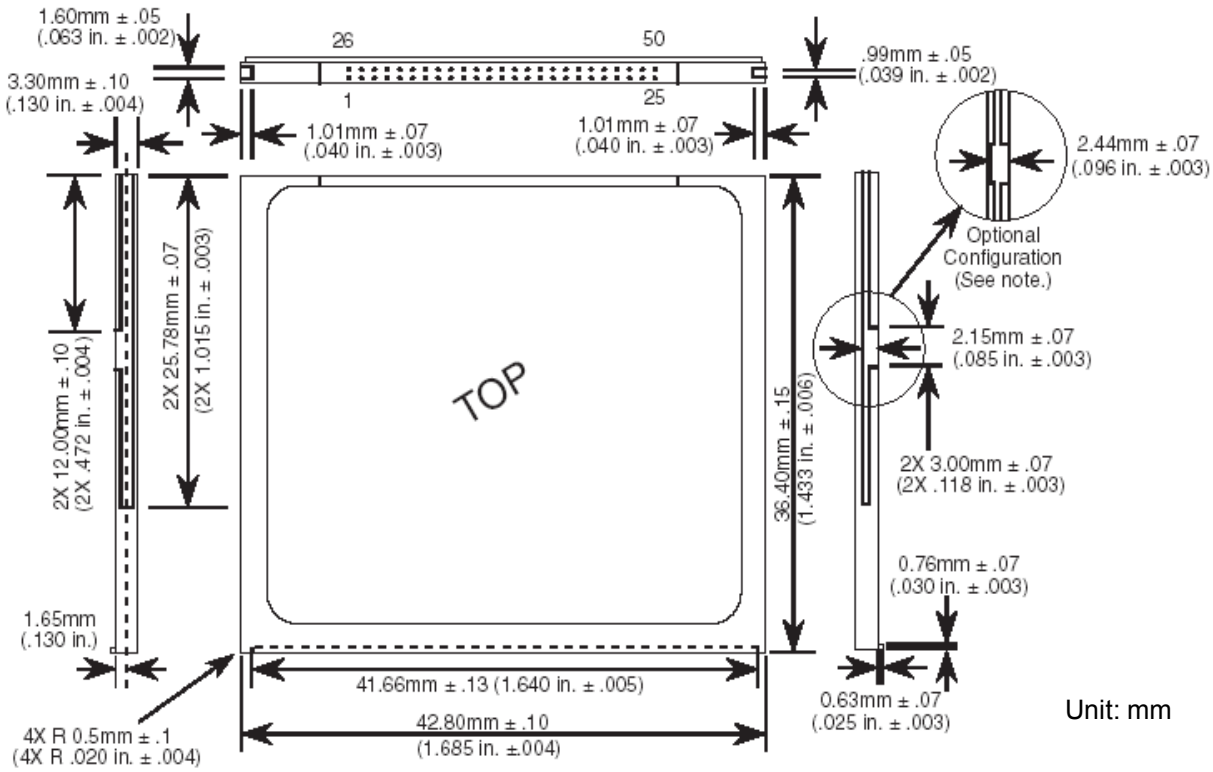

FIGURE 8-1: Physical dimension

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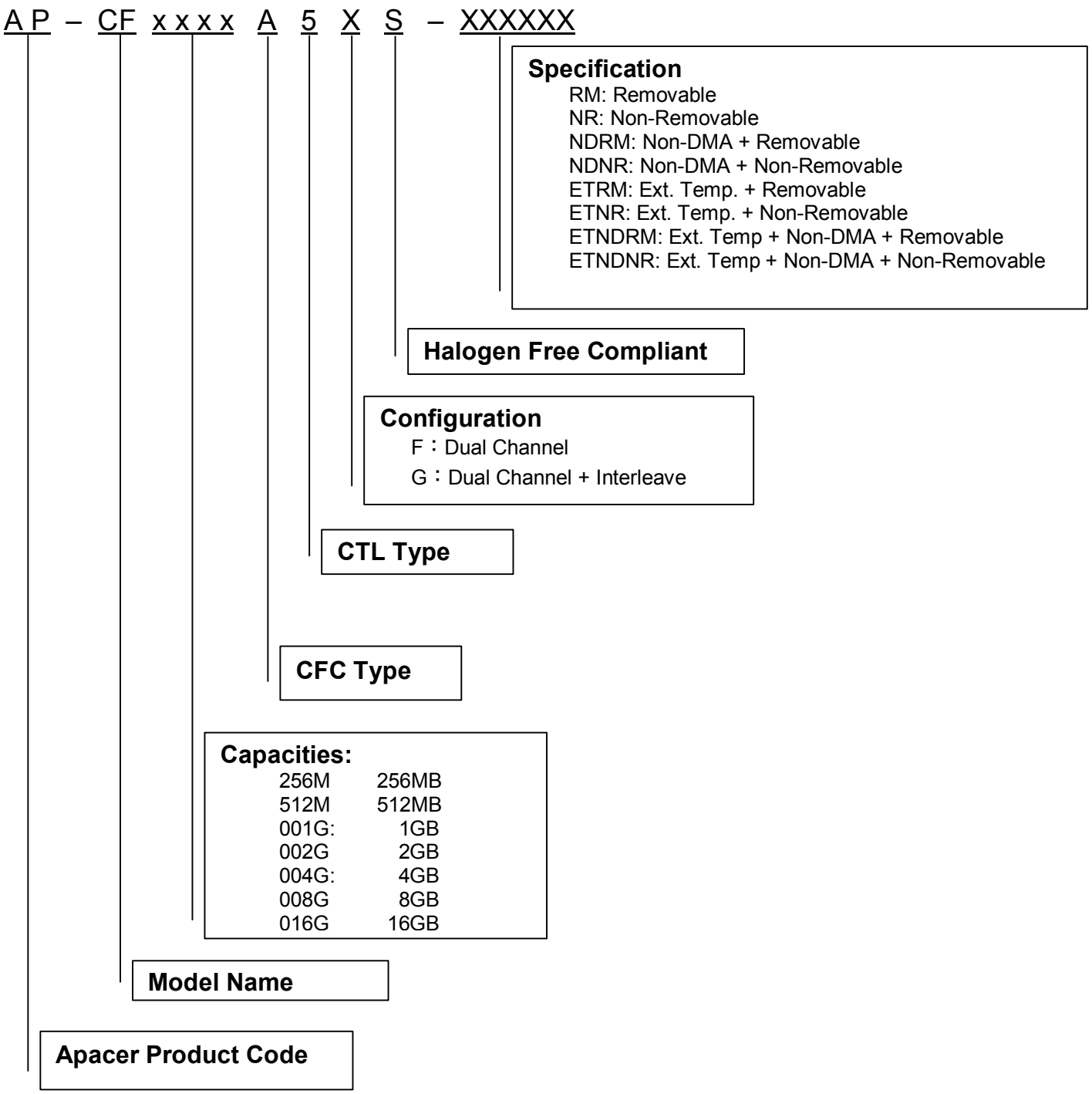
9. Product Ordering Information

9.1 Product Code Designations



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9.2 Valid Combinations

9.2.1 Standard Temperature

- **9.2.1.1 Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-RM
512MB	AP-CF512MA5GS-RM
1GB	AP-CF001GA5GS-RM
2GB	AP-CF002GA5GS-RM
4GB	AP-CF004GA5GS-RM
8GB	AP-CF008GA5GS-RM
16GB	AP-CF016GA5GS-RM

- **9.2.1.2 Non-Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-NR
512MB	AP-CF512MA5GS-NR
1GB	AP-CF001GA5GS-NR
2GB	AP-CF002GA5GS-NR
4GB	AP-CF004GA5GS-NR
8GB	AP-CF008GA5GS-NR
16GB	AP-CF016GA5GS-NR

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- **9.2.1.3 Non-DMA + Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-NDRM
512MB	AP-CF512MA5GS-NDRM
1GB	AP-CF001GA5GS-NDRM
2GB	AP-CF002GA5GS-NDRM
4GB	AP-CF004GA5GS-NDRM
8GB	AP-CF008GA5GS-NDRM
16GB	AP-CF016GA5GS-NDRM

- **9.2.1.4 Non-DMA + Non-Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-NDNR
512MB	AP-CF512MA5GS-NDNR
1GB	AP-CF001GA5GS-NDNR
2GB	AP-CF002GA5GS-NDNR
4GB	AP-CF004GA5GS-NDNR
8GB	AP-CF008GA5GS-NDNR
16GB	AP-CF016GA5GS-NDNR

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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9.2.2 Extended Temperature

- **9.2.2.1 Ext. Temp. + Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-ETRM
512MB	AP-CF512MA5GS-ETRM
1GB	AP-CF001GA5GS-ETRM
2GB	AP-CF002GA5GS-ETRM
4GB	AP-CF004GA5GS-ETRM
8GB	AP-CF008GA5GS-ETRM
16GB	AP-CF016GA5GS-ETRM

- **9.2.2.2 Ext. Temp. + Non-Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-ETNR
512MB	AP-CF512MA5GS-ETNR
1GB	AP-CF001GA5GS-ETNR
2GB	AP-CF002GA5GS-ETNR
4GB	AP-CF004GA5GS-ETNR
8GB	AP-CF008GA5GS-ETNR
16GB	AP-CF016GA5GS-ETNR

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- **9.2.2.3 Ext. Temp. + Non-DMA + Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-ETNDRM
512MB	AP-CF512MA5GS-ETNDRM
1GB	AP-CF001GA5GS-ETNDRM
2GB	AP-CF002GA5GS-ETNDRM
4GB	AP-CF004GA5GS-ETNDRM
8GB	AP-CF008GA5GS-ETNDRM
16GB	AP-CF016GA5GS-ETNDRM

- **9.2.2.4 Ext. Temp. + Non-DMA + Non-Removable**

Capacity	*AP/N*
256MB	AP-CF256MA5FS-ETNDNR
512MB	AP-CF512MA5GS-ETNDNR
1GB	AP-CF001GA5GS-ETNDNR
2GB	AP-CF002GA5GS-ETNDNR
4GB	AP-CF004GA5GS-ETNDNR
8GB	AP-CF008GA5GS-ETNDNR
16GB	AP-CF016GA5GS-ETNDNR

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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Revision History

Revision	Date	Description	Remark
1.0	11/17/2009	Official release	

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