RoHS Compliant

Value Added Compact Flash Series Ⅲ

Specification for Industrial CF

February 11, 2009

Version 1.2

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Features:

- **Compact Flash Association Specification Revision 3.0 Standard Interface**
  - ATA command set compatible
  - ATA mode support for up to:
    PIO Mode-6
    Multiword DMA Mode-4
    Ultra DMA Mode-4
- **Connector Type**
  - 50 pins female
- **Low power consumption (typical)**
  - Supply voltage: 3.3V & 5V
  - Active mode: 80 mA/95 mA (3.3V/5.0V)
  - Sleep mode: 700 µA/900 µA (3.3V/5.0V)
- **Performance**
  - Sustained read: up to 35 MB/sec
  - Sustained write:
    Standard: up to 15 MB/sec
    High Speed: up to 25 MB/sec
- **Capacity**
  - Standard:
    128, 256, 512 MB
    1, 2, 16 GB
  - High Speed:
    256, 512 MB
    1, 2, 4, 8 GB
- **NAND flash type: SLC**
- **Temperature ranges**
  - Operation:
    Standard: 0℃ to 70℃
    ET[1]: -40℃ to 85℃
  - Storage: -40℃ to 100℃
- **Flash management**
  - Intelligent endurance design
    Advanced wear-leveling algorithms
    S.M.A.R.T. Technology
    Built-in Hardware ECC
    Enhanced Data Integrity
  - Intelligent power failure recovery
- **RoHS compliant**

1. Extended Temperature

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1. General Description

Apacer's Industrial Compact Flash Card (CFC) offers the most reliable and high performance storage which is compatible with CF Type I and Type II devise. Unlike the ordinary consumer Compact Flash cards, Apacer Industrial Compact Flash card provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's CFC provides complete PCMCIA - ATA functionality and compatibility. Apacer 's Compact Flash technology is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

Featuring technologies as Advanced Wear-leveling algorithms, S.M.A.R.T, Enhanced Data Integrity, Built-in Hardware ECC, and Intelligent Power Failure Recovery, Apacer's Industrial Compact Flash Card assures users of a versatile device on data storage.

1.1 Performance-Optimized Controller

The Compact Flash Card Controller translates standard CF signals into flash media data and control signals.

1.1.1 Power Management Unit (PMU)

The power management unit (PMU) controls the power consumption of the Compact Flash card controller. It reduces the power consumption of the Compact Flash Card Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

1.1.2 SRAM Buffer

The Compact Flash Card Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

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2. Functional Block

The Compact Flash Card (CFC) includes a controller and flash media, as well as the Compact Flash standard interface. Figure 2-1 shows the functional block diagram.

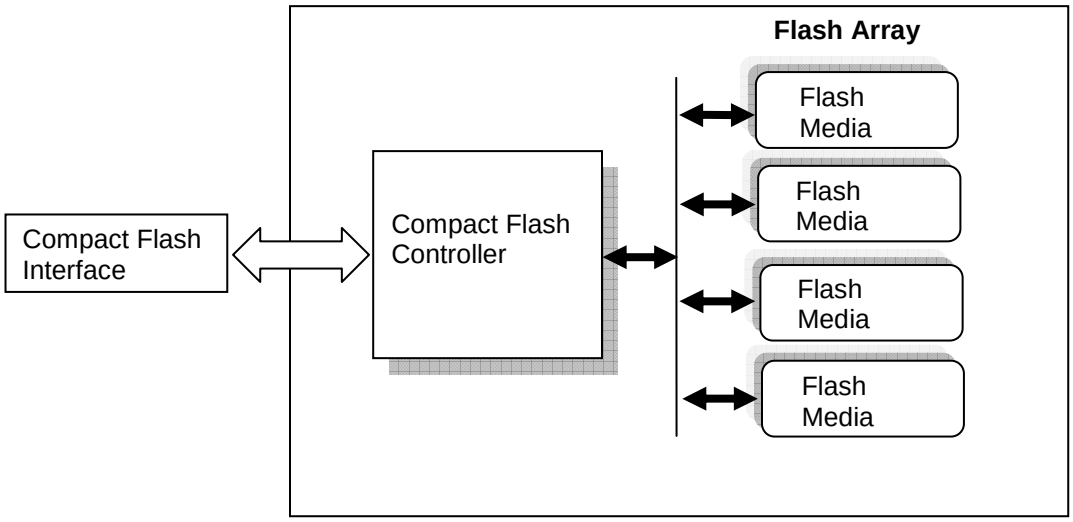

Figure 2-1: Functional block diagram

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3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1: Pin assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CE1	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#OE	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOCS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CE2	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	RESET	I

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Table 3-1: Pin assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	-REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	O
46	BVD1	O	#STSCHG	O	#PDIAG	O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be tied to VCC by the host.
2. Connection required when UDMA is in use.

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4. Capacity Specification

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Max LBA
128 MB	127,641,600	980	8	32	250,880
256 MB	256,352,256	980	16	32	501,760
512 MB	511,664,128	993	16	63	1,000,944
1GB	1,024,655,360	1,986	16	63	2,001,888
2GB	2,048,589,824	3,970	16	63	4,001,760
4GB	4,100,059,136	7,964	16	63	8,027,712
8GB	8,176,340,992	15,880	16	63	16,007,040
16GB	16,368,721,920	16,383*	16	63	32,014,080

1. Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

4.1 Performance Specification

Performances of the Standard and High Speed ATA-Flash Disk are listed in Table 4-2 and Table 4-3.

Table 4-2: Standard Performance specifications

Capacity / Performance	128 MB / 256 MB	512 MB / 1 GB	2 GB	16 GB
Sustained read (MB/s)	18	30	35	22
Sustained write (MB/s)	7	12	15	15

Table 4-3: High Speed Performance specifications

Capacity / Performance	256 MB / 512 MB	1GB / 2 GB / 4 GB / 8 GB
Sustained read (MB/s)	30	35
Sustained write (MB/s)	13	22~25

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4.2 Environmental Specifications

Environmental specification of the Compact Flash Card series (CFC) which follows the MIL-STD-810F standards is available as shown in Table 4-4.

Table 4-4: Environmental specifications

Environment		Specification
Temperature	Operation	0℃ to 70℃; -40℃ to 85℃ (ET [1])
	Storage	-40℃ to 100℃
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

1. Extended Temperature

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5. Flash Management

5.1 Intelligent Endurance Design

5.1.1 Advanced wear-leveling algorithms

The NAND flash devices are limited by a certain number of write cycles. When using a file system, frequent file table updates is mandatory. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole device, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. The scheme is achieved both via buffer management and Apacer-specific advanced wear leveling to ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

5.1.2 S.M.A.R.T. technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

5.1.3 Built-in hardware ECC

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.1.4 Enhanced data integrity

The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms and bad block management. Flash controllers can support up to 8 bits ECC capability for accuracy of data transactions, and bad block management is a preventive mechanism from loss of data by retiring unusable media blocks and relocating the data to the other blocks, along with the integration of advanced wear leveling algorithms, so that the lifespan of device can be expanded.

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5.2 Intelligent Power Failure Recovery

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

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6. Software Interface

6.1 Command Set

Table 6-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: Command set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
Flush-Cache	E7H	-	-	-	-	D	-
Format Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Request-Sense	03H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y[7]	-	-	-	D	-

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Table 6-1: Command set (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
SMART	B0H	Y	Y	Y	Y	D	
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Translate-Sector	87H	-	Y	Y	Y	Y	Y
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDH	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector-Without-Erase	38H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder registers
5. DH - Drive/Head register
6. LBA - Logical Block Address mode supported (see command descriptions for use)
7. Y - The register contains a valid parameter for this command
8. For the Drive/Head register:
Y means both the CFC and Head parameters are used
D means only the CFC parameter is valid and not the Head parameter

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7. Electrical Specification

Caution: **Absolute Maximum Stress Ratings –** Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Range	Ambient Temperature	3.3V	5V
Standard	0℃ to +70℃	3.135-3.465V	4.75-5.25V
Extended Temperature	-40℃ to +85℃		

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to VDD + 0.5V max.

Table 7-3: Recommended system power-up timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-READY}$[1]	Power-up to Ready Operation	200	1000	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	200	1000	ms

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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8. Physical Characteristics

8.1 Dimension

TABLE 8-1: Type I CFC physical specification

Length:	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
Width:	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
Thickness (Including Label Area):	3.3mm+/-0.10mm (0.130+/-0.04in.)

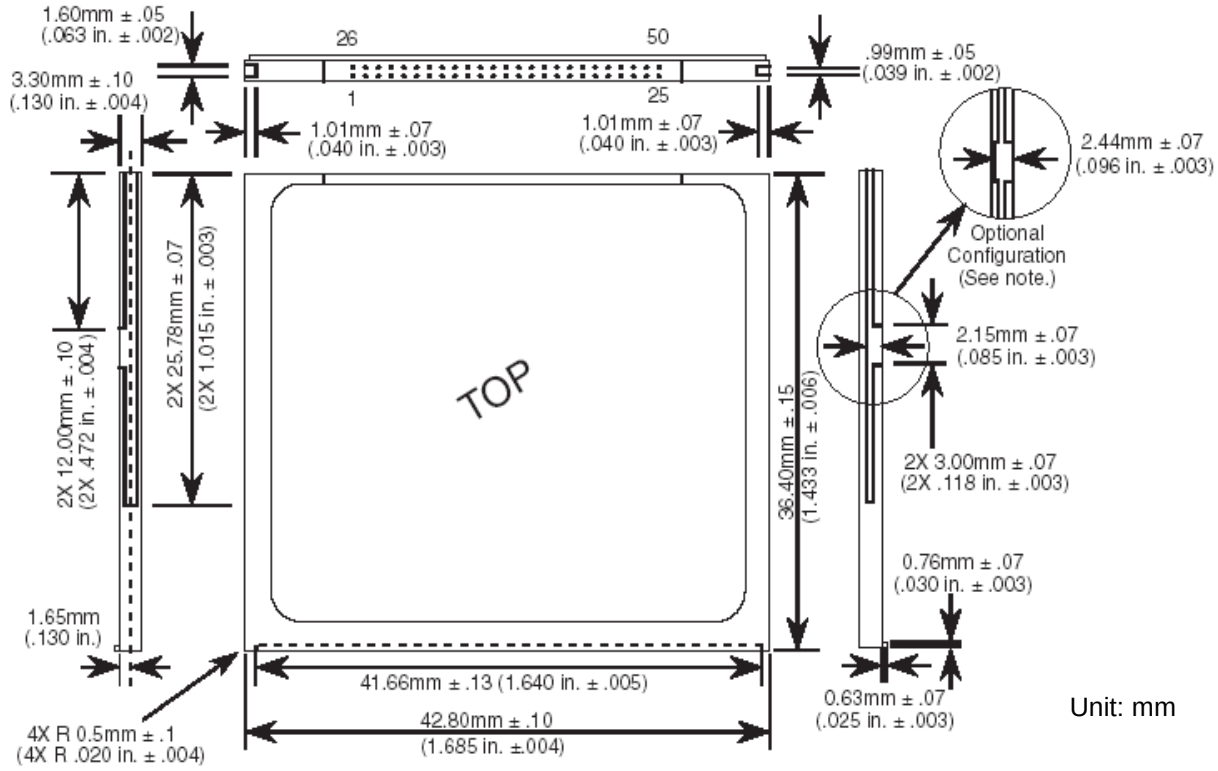

FIGURE 8-1: Physical dimension

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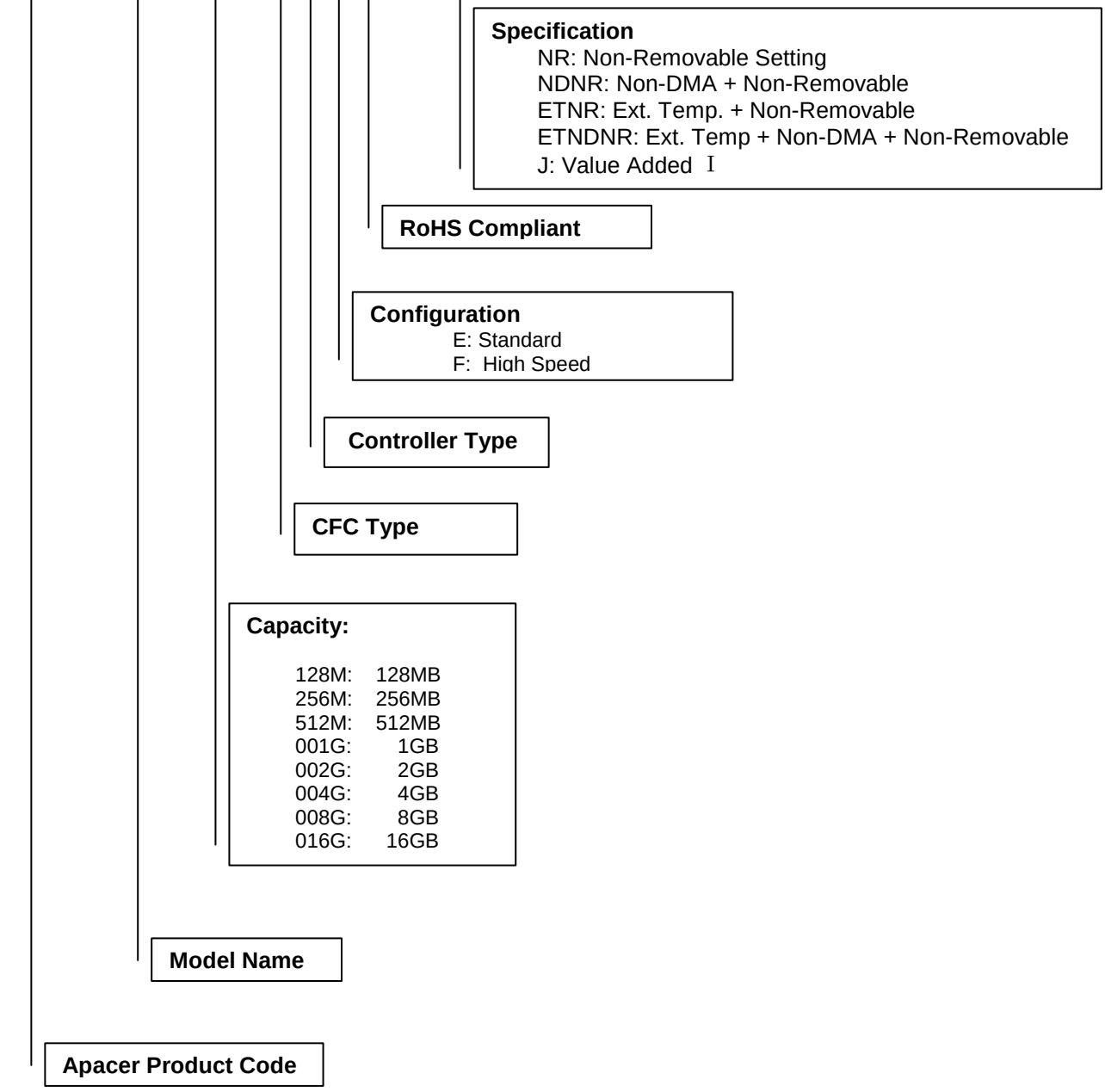
9. Product Ordering Information

9.1 Product Code Designations

A P – C F x x x x E 3 X R – XXXXJ



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9.2 Valid Combinations

Standard Temperature

Non-Removable

Standard **High Speed**

Capacity	P/N	Capacity	P/N
128MB	AP-CF128ME3ER-NRJ	256MB	AP-CF256ME3FR-NRJ
256MB	AP-CF256ME3ER-NRJ	512MB	AP-CF512ME3FR-NRJ
512MB	AP-CF512ME3ER-NRJ	1GB	AP-CF001GE3FR-NRJ
1GB	AP-CF001GE3ER-NRJ	2GB	AP-CF001GE3FR-NRJ
2GB	AP-CF002GE3ER-NRJ	4GB	AP-CF004GE3FR-NRJ
16GB	AP-CF016GE3ER-NRJ	8GB	AP-CF008GE3FR-NRJ

Non-DMA & Non-Removable

Standard **High Speed**

Capacity	P/N	Capacity	P/N
128MB	AP-CF128ME3ER-NDNRJ	256MB	AP-CF256ME3FR-NDNRJ
256MB	AP-CF256ME3ER-NDNRJ	512MB	AP-CF512ME3FR-NDNRJ
512MB	AP-CF512ME3ER-NDNRJ	1GB	AP-CF001GE3FR-NDNRJ
1GB	AP-CF001GE3ER-NDNRJ	2GB	AP-CF001GE3FR-NDNRJ
2GB	AP-CF002GE3ER-NDNRJ	4GB	AP-CF004GE3FR-NDNRJ
16GB	AP-CF016GE3ER-NDNRJ	8GB	AP-CF008GE3FR-NDNRJ

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Extended Temperature

Non-Removable

Standard

Capacity	P/N
128MB	AP-CF128ME3ER-ETNRJ
256MB	AP-CF256ME3ER-ETNRJ
512MB	AP-CF512ME3ER-ETNRJ
1GB	AP-CF001GE3ER-ETNRJ
2GB	AP-CF002GE3ER-ETNRJ
16GB	AP-CF016GE3ER-ETNRJ

High Speed

Capacity	P/N
256MB	AP-CF256ME3FR-ETNRJ
512MB	AP-CF512ME3FR-ETNRJ
1GB	AP-CF001GE3FR-ETNRJ
2GB	AP-CF001GE3FR-ETNRJ
4GB	AP-CF004GE3FR-ETNRJ
8GB	AP-CF008GE3FR-ETNRJ

Non-DMA & Non-Removable

Standard

Capacity	P/N
128MB	AP-CF128ME3ER-ETNDNRJ
256MB	AP-CF256ME3ER-ETNDNRJ
512MB	AP-CF512ME3ER-ETNDNRJ
1GB	AP-CF001GE3ER-ETNDNRJ
2GB	AP-CF002GE3ER-ETNDNRJ
16GB	AP-CF016GE3ER-ETNDNRJ

High Speed

Capacity	P/N
256MB	AP-CF256ME3FR-ETNDNRJ
512MB	AP-CF512ME3FR-ETNDNRJ
1GB	AP-CF001GE3FR-ETNDNRJ
2GB	AP-CF001GE3FR-ETNDNRJ
4GB	AP-CF004GE3FR-ETNDNRJ
8GB	AP-CF008GE3FR-ETNDNRJ

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Revision History

Revision	Date	Description	Remark
1.0	12/30/2008	Official release	
1.1	01/08/2009	Context revised	
1.2	02/11/2009	Modified document layout	

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